

[REDACTED]

**PLASTIC**  
**MRTL**  
**INTEGRATED CIRCUITS**  
**LOW-POWER**  
**AND**  
**MEDIUM-POWER**  
**MC700P/MC800P SERIES**

[REDACTED]

# PLASTIC MRTL

## INTEGRATED CIRCUITS

## General Information

### Summary of Devices Available in mW MRTL (low power)

### Summary of Devices Available in MRTL (medium power)

## POWER

MC715P, MC815P	Dual 3-Input Gates	MRTL
— MC816P	J-K Flip-Flop (see MC723P)	MRTL
MC717P, MC817P	Quad 2-Input Gates	mW MRTL
MC718P, MC818P	Dual 3-Input Gates	mW MRTL
MC719P, MC819P	Dual 4-Input Gates	mW MRTL
MC722P, MC822P	J-K Flip-Flops	mW MRTL
MC723P, MC816P	J-K Flip-Flops	MRTL
MC724P, MC824P	Quad 2-Input Gates	MRTL
MC725P, MC825P	Dual 4-Input Gates	MRTL
MC726P, MC826P	J-K Flip-Flops	MRTL
MC764P, MC864P	Dual Exclusive OR-NOR Gate	mW MRTL
MC767P, MC867P	Quad Latch	mW MRTL
MC770P, MC870P	BCD-to-Decimal Decoder	mW MRTL
MC771P, MC871P	Quad Exclusive OR Gates	MRTL
MC775P, MC875P	Dual Half-Adders	MRTL
MC776P, MC876P	Dual J-K Flip-Flops	mW MRTL
MC777P, MC877P	Binary Up Counter	MRTL
MC778P, MC878P	Dual Type D Flip-Flops	mW MRTL
MC779P, MC879P	1 J-K Flip-Flop, 1 Expander, 2 Buffers	MRTL
MC780P, MC880P	Decade Up Counter	MRTL
MC783P, MC883P	Dual Half-Shift Registers With Inverter	MRTL
MC784P, MC884P	Dual Half-Shift Registers	MRTL
MC785P, MC885P	Quad 2-Input Expanders	MRTL
MC786P, MC886P	Dual 4-Input Expanders	MRTL
MC787P, MC887P	1 J-K Flip-Flop, 1 Inverter, 2 Buffers	MRTL
MC788P, MC888P	Dual Buffers, Non-Inverting	MRTL
MC789P, MC889P	Hex Inverters	MRTL
MC790P, MC890P	Dual J-K Flip-Flops	MRTL
MC791P, MC891P	Dual J-K Flip-Flops	MRTL
MC792P, MC892P	Triple 3-Input Gates	MRTL
MC793P, MC893P	Triple 3-Input Gates	mW MRTL
MC794P, MC894P	Serial-Parallel Shift Register	MRTL
MC796P, MC896P	Dual Full Adders	MRTL
MC797P, MC897P	Dual Full Subtractors	MRTL
MC798P, MC898P	Dual Buffers	mW MRTL
MC799P, MC899P	Dual Buffers, Inverting	MRTL
MC9701P, MC9801P	Dual 4-Channel Data Selector	MRTL
MC9704P, MC9804P	4-Bit Parallel Full Adder	MRTL
MC9707P, MC9807P	Dual 4-Channel Data Distributor	MRTL
MC9709P, MC9809P	Quad Schmitt Trigger	MRTL
MC9713P, MC9813P	Quad 2-Input AND Gate	MRTL
MC9714P, MC9814P	Quad 2-Input NAND Gate	MRTL
MC9715P, MC9815P	Quad 2-Input OR Gate	MRTL
MC9718P, MC9818P	Hex Inverter	mW MRTL
MC9719P, MC9819P	Hex Expanders	MRTL
MC9720P, MC9820P	Hex Expander	mW MRTL
MC9721P, MC9821P	Quad 2-Input Expanders	mW MRTL
MC9722P, MC9822P	Dual J-K Flip-Flop	mW MRTL
MC9760P, MC9860P	BCD-to-Decimal Decoder Driver	MRTL

## FUNCTIONS AND CHARACTERISTICS

### MRTL

$V_{CC} = 3.6 \text{ V} \pm 10\%$ ,  $T_A = 25^\circ\text{C}$

Function	Type		Case	Output Loading Factor Each Output		Propagation Delay	Total Power Dissipation
	+15 to +55°C	0 to +75°C		mW MRTL	MRTL	$t_{pd}$ ns typ	

#### GATES

Dual 3-Input Gates	MC715P	MC815P	605	16	5	12	55/15 ②
Quad 2-Input Gates	MC724P	MC824P	605	16	5	12	100/30 ②
Dual 4-Input Gates	MC725P	MC825P	605	16	5	12	60/15 ②
Quad Exclusive OR Gates	MC771P	MC871P	605	16	5	12	87
Triple 3-Input Gates	MC792P	MC892P	605	16	5	12	82/24 ②
Quad 2-Input AND Gate	MC9713P	MC9813P	605	16	5	28	100
Quad 2-Input NAND Gate	MC9714P	MC9814P	605	16	5	14 ⑤	145
Quad 2-Input OR Gate	MC9715P	MC9815P	605	16	5	14 ⑤	28/100 ②

#### BUFFERS

Dual Buffers, Non-Inverting	MC788P	MC888P	605	80	25	24	145/56 ②
Dual Buffers, Inverting	MC799P	MC899P	605	80	25	20	50/100 ②

#### FLIP-FLOPS

J-K Flip-Flops	—	MC816P	605	—	3	35	91/79 ③
J-K Flip-Flops	MC723P	—	605	10	—	35	91/79 ③
J-K Flip-Flops	MC726P	MC826P	605	16	5	35	100/86 ③
Dual J-K Flip-Flops	MC790P	MC890P	605	10	3	35	182/158 ③
Dual J-K Flip-Flops	MC791P	MC891P	605	16	5	40	190/160 ③

#### INVERTER

Hex Inverters	MC789P	MC899P	605	16	5	12	130/15 ②
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#### EXPANDERS

Quad 2-Input Expanders	MC785P	MC885P	605	—	—	12	20/- ②
Dual 4-Input Expanders	MC786P	MC886P	605	—	—	12	20/- ②
Hex Expanders	MC9719P	MC9819P	605	—	—	12	13/- ②

#### MULTI-FUNCTION DEVICES

1 J-K Flip-Flop, 1 Expander, 2 Buffers	MC779P	MC879P	605	—	—	—	141/124 ④
1 J-K Flip-Flop, 1 Inverter, 2 Buffers	MC787P	MC887P	605	—	—	—	138/132 ④

#### ADDERS AND SUBTRACTORS

Dual Half-Adders	MC775P	MC875P	605	16	5	20	120
Dual Full Adders	MC796P	MC896P	605	16	5	60	225
Dual Full Subtractors	MC797P	MC897P	605	16	5	60	225
4-Bit Parallel Full Adder	MC9704P	MC9804P	612	6	2	125	265

#### SHIFT REGISTERS

Dual Half-Shift Registers With Inverter	MC783P	MC883P	605	13	4	22	140
Dual Half-Shift Registers	MC784P	MC884P	605	13	4	22	100
Serial-Parallel Shift Register	MC794P	MC894P	605	16	5	55	225

#### COUNTERS

Binary Up Counter	MC777P	MC877P	605	10	3	—	180
Decade Up Counter	MC780P	MC880P	605	10	3	—	250

#### DATA ROUTING FUNCTION

Dual 4-Channel Data Selector	MC9701P	MC9801P	612	16	5	25	100
Dual 4-Channel Data Distributor	MC9707P	MC9807P	612	16	5	25	150

#### SCHMITT TRIGGER

Quad Schmitt Trigger	MC9709P	MC9809P	605	16	5	30	95
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#### DECODER/DRIVER

BCD-to-Decimal Decoder Driver	MC9760P	MC9860P	612	—	—	—	115
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**FUNCTIONS AND CHARACTERISTICS (continued)**  
mW MRTL

Function	Type		Case	Output Loading Factor Each Output	Propagation Delay t <sub>pd</sub> ns typ	Total Power Dissipation mW typ/pkg
	+15 to +55°C	0 to +75°C		Medium and Low Power		

**GATES**

Quad 2-Input Gates	MC717P	MC817P	605	4	27	20/5.0 ②
Dual 3-Input Gates	MC718P	MC818P	605	4	27	12/2.5 ②
Dual 4-Input Gates	MC719P	MC819P	605	4	27	13/2.5 ②
Dual Exclusive OR-NOR Gate	MC764P	MC864P	605	3,4	35,65	25
Triple 3-Input Gates	MC793P	MC893P	605	4	27	18/3.5 ②

**FLIP-FLOPS**

J-K Flip-Flops	MC722P	MC822P	605	4	70	24/20 ③
Quad Latch	MC767P	MC867P	612	9	50	110
Dual J-K Flip-Flops	MC776P	MC876P	605	2	50	41/29 ③
Dual Type D Flip-Flops	MC778P	MC878P	605	3	60	48/35 ①
Dual J-K Flip-Flop	MC9722P	MC9822P	605	4	75	24/- ③

**BUFFER**

Dual Buffers	MC798P	MC898P	605	30	57	14/46 ②
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**INVERTERS**

Hex Inverter	MC9718P	MC9818P	605	4	27	7.0/3.0 ②
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**EXPANDERS**

Hex Expander	MC9720P	MC9820P	605	—	12	30/- ②
Quad 2-Input Expanders	MC9721P	MC9821P	605	—	27	20/- ②

**DECODER**

BCD-to-Decimal Decoder	MC770P	MC870P	612	7	36	100/- ②
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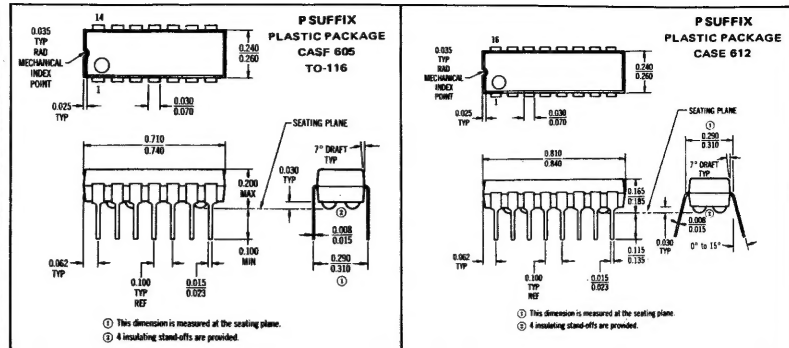
- ① Direct Set and Direct Clear Low, All other Inputs High/All Inputs Low.  
 ② Inputs High/Inputs Low  
 ③ Only Clock Inputs High/Inputs Low  
 ④ Only Clock Input high on flip-flop, other element Inputs High/Inputs Low  
 ⑤ Operating frequency (MHz)

## GENERAL INFORMATION

## PLASTIC MRTL MC700P/800P series

### PACKAGING

Plastic MRTL 14-lead devices are in Case 605 (TO-116); 16-lead devices are in Case 612.



### MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$

Rating	Symbol	Value	Unit
Input Voltage	—	$\pm 4.0$	Vdc
Power Supply Voltage (Pulsed $\leq 1.0$ s)	—	+12	Vdc
Operating Temperature Range MC700P Series MC800P Series	$T_A$	+15 to +55 0 to +75	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-55 to +125	$^\circ\text{C}$

### TEST CONDITION TOLERANCES

$$V_{BOT} = \pm 10 \text{ mV} \quad V_{CC} = \pm 10 \text{ mV} \quad V_{in} = \pm 2 \text{ mV} \quad V_R = \pm 1\% \quad V_{on} = \pm 2 \text{ mV} \quad V_{off} = \pm 2 \text{ mV} \quad V_{LL} = \pm 2 \text{ mV}$$

### DEFINITIONS

$I_{A2}, I_{A3}, I_{A4}, I_{A5}, I_{A10}, I_{A13}, I_{A16}$	Minimum available output current from a device with an output loading factor of 2, 3, 4, 5, 10, 13, and 16 respectively. Output voltage not to fall below the value of $V_{in}$ .
$I_{A3}$	Minimum available output current from a buffer. Output voltage not to fall below the value of $V_{on}$ .
$I_{AM}$	The maximum available current from the output of a Dual Gate.
$I_{CEX}$	Collector current of a circuit when $V_{in}$ is applied to the output pin and $V_{off}$ is applied to the input pins.
$I_{in}$	Maximum input current drawn by one input of a gate with $V_{in}$ applied. All other gate inputs are returned to $V_{BOT}$ .
1.8 $I_{in}$	Current drawn from the $V_{in}$ supply by the Toggle pin of the Flip-Flop.
2 $I_{in}$	Maximum input current drawn by one input of a device with 2 bases internally tied together.
$I_L$	Isolation leakage current.

$I_o$	Output load current.
$V_{BOT}$	A high value voltage applied to an input of a device to insure saturation of the driven transistor.
$V_{CC}$	Supply voltage.
$V_{CE(sat)}$	Maximum saturation voltage with $V_{BOT}$ applied to the input.
$V_{in}$	Minimum high level voltage applied to the input of a device.
$V_{LL}$	A supply voltage low enough to allow flow of leakage currents only.
$V_{off}$	The maximum voltage which may be applied to an input terminal without turning the transistor on.
$V_{on}$	The minimum voltage which may be applied to an input terminal that will turn the transistor on.
$V_{out}$	The maximum output voltage with $V_{on}$ applied to the input.
$V_R$	Value of external resistor connected to $V_{CC}$ for test purposes. $V_{RH}$ = highest node resistor value $V_{RL}$ = lowest node resistor value

### GENERAL RULES

#### EXPANDER RULES:

- The MC785P/885P, MC786P/886P and MC9719P/9819P MRTL expanders can be used to expand medium-power MRTL output nodes only. The MC9721P/9821P expander can be used to expand mW MRTL output nodes only.
  - mW MRTL and MC800 MRTL Series: When using the MC885P, MC886P, MC9819P or MC9721/9821 subtract 0.5 from the output loading factor of the expanded gate for each expander node that is connected; also increase the input loading factor of the expanded gate by a factor of 1.33.
  - MC700 MRTL Series: When using the MC785P, MC786P or MC9719P subtract 2.0 from the output loading factor of the medium-power MRTL expanded gate for each expander node that is connected; also increase the input loading factor of the medium-power expanded gate by a factor of 3.75.
- The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output.
  - When mixing MRTL and mWMRTL in the same system, the loading factors must be normalized in accordance with the input current of the units being driven.
  - All unused inputs should be returned to ground.

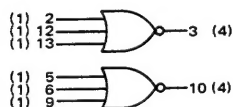
# LOW-POWER mW MRTL DEVICES

The logic diagrams shown describe the MC700P/MC800P Series of low-power resistor-transistor logic integrated circuits and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time ( $t_{pd}$ ), typical package power dissipation ( $P_D$ ), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (if on the circuit input terminal) or load driving ability – fan-out – (if on the circuit output terminal).

Using the indicated loading factors, these low-power mW MRTL circuits are compatible with the medium-power MRTL circuits shown in this section. The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. The loading data is valid over the temperature range of +15 to +55°C for the MC700P Series, and 0 to +75°C for the MC800P Series, with  $V_{CC} = 3.6 V \pm 10\%$ .

## GATES

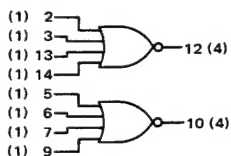
**MC718P • MC818P**  
Dual 3-Input Gate



$$3 = \overline{2 + 12 + 13}$$

$t_{pd} = 27 \text{ ns}$   
 $P_D = 12 \text{ mW (Input High)}$   
 $2.5 \text{ mW (Inputs Low)}$

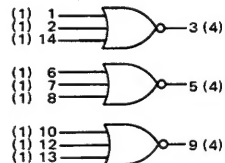
**MC719P • MC819P**  
Dual 4-Input Gate



$$12 = \overline{2 + 3 + 13 + 14}$$

$t_{pd} = 27 \text{ ns}$   
 $P_D = 13 \text{ mW (Input High)}$   
 $2.5 \text{ mW (Inputs Low)}$

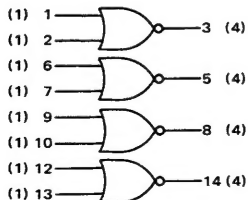
**MC793P • MC893P**  
Triple 3-Input Gate



$$3 = \overline{1 + 2 + 14}$$

$t_{pd} = 27 \text{ ns}$   
 $P_D = 18 \text{ mW (Input High)}$   
 $3.5 \text{ mW (Inputs Low)}$

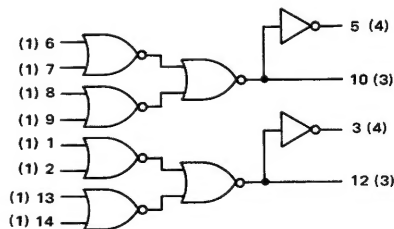
**MC717P • MC817P**  
Quad 2-Input Gate



$$3 = \overline{1 + 2}$$

$t_{pd} = 27 \text{ ns}$   
 $P_D = 20 \text{ mW (Input High)}$   
 $5.0 \text{ mW (Inputs Low)}$

**MC764P • MC864P**  
Dual Exclusive OR-NOR Gate



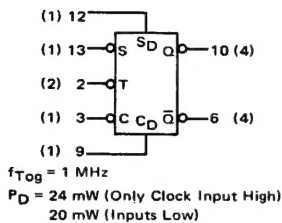
$$12 = \overline{(1 + 2) \cdot (13 + 14)}$$

$$3 = \overline{1 \cdot 2 + 13 \cdot 14}$$

$t_{pd} = 65 \text{ ns (Pins 5 and 3)}$   
 $t_{pd} = 35 \text{ ns (Pins 10 and 12)}$   
 $P_D = 25 \text{ mW}$

FLIP-FLOPS

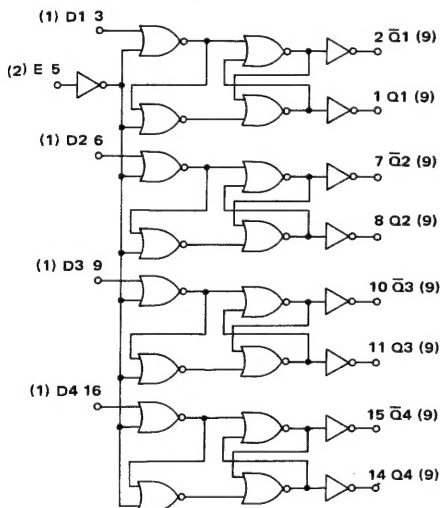
MC722P • MC822P  
J-K Flip-Flop



DIRECT INPUT OPERATION ①				CLOCKED INPUT OPERATION ③			
S <sub>D</sub>	C <sub>D</sub>	Q	$\bar{Q}$	t <sub>n</sub> ④	t <sub>n+1</sub> ④	Q	$\bar{Q}$
0	0	②	②	S	C	Q <sub>n</sub> ⑤	$\bar{Q}_n$
1	0	1	0	1	1	1	0
0	1	0	1	1	0	0	1
1	1	0	0	0	0	$\bar{Q}_n$	Q <sub>n</sub> ⑤

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from S<sub>D</sub> = C<sub>D</sub> to S<sub>D</sub> = C<sub>D</sub> = 0. The output state cannot be predetermined in the case where the input goes from S<sub>D</sub> = C<sub>D</sub> = 1 to S<sub>D</sub> = C<sub>D</sub> = 0.
3. Direct inputs (C<sub>D</sub> and S<sub>D</sub>) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t<sub>n</sub> and the time period subsequent to this transition is denoted t<sub>n+1</sub>.
5. Q<sub>n</sub> is the state of the Q output in the time period t<sub>n</sub>.
6. Clock pulse fall time must be < 100 ns.

MC767P • MC867P  
Quad Latch



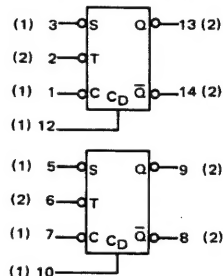
t<sub>pd(avg)\*</sub> = 50 ns typ  
P<sub>D</sub> = 110 mW typ

$$* \text{Avg } t_{pd} = \frac{t_{on} + t_{off}}{2}$$

TRUTH TABLE

E	D	Q <sub>n+1</sub>	$\bar{Q}_{n+1}$
0	0	Q <sub>n</sub>	$\bar{Q}_n$
0	1	Q <sub>n</sub>	$\bar{Q}_n$
1	0	0	1
1	1	1	0

MC776P • MC876P  
Dual J-K Flip-Flop



f<sub>Tog</sub> = 3 MHz  
P<sub>D</sub> = 41 mW (Only Clock Input High)  
29 mW (Inputs Low)

CLOCKED INPUT OPERATION

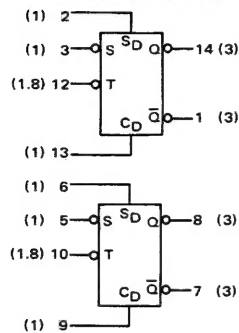
t <sub>n</sub>		t <sub>n+1</sub>	
S	C	Q	$\bar{Q}$
1	1	Q <sub>n</sub>	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q <sub>n</sub>

1. Direct input (C<sub>D</sub>) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t<sub>n</sub> and the time period subsequent to this transition is denoted t<sub>n+1</sub>.
3. Q<sub>n</sub> is the state of the Q output in the time period t<sub>n</sub>.
4. Clock pulse fall time must be < 100 ns.

LOW-POWER mW MRTL DEVICES (continued)

FLIP-FLOPS (continued)

MC778P • MC878P  
Dual Type D Flip-Flop

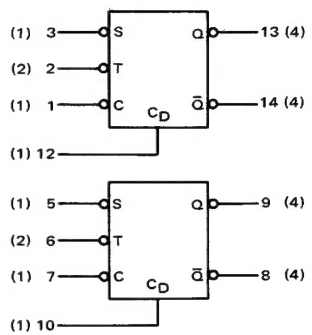


$f_{Tog} = 1 \text{ MHz}$   
 $P_D = 48 \text{ mW}$  (Direct Set ( $S_D$ ) and Direct Clear ( $C_D$ ) Low; all other Inputs High)  
35 mW (All Inputs Low)

DIRECT INPUT OPERATION ①				CLOCKED INPUT OPERATION ③			
$S_D$	$C_D$	Q	$\bar{Q}$	$t_n$ ②	$t_{n+1}$ ②	Q	$\bar{Q}$
0	0	②	②	S	Q	$\bar{Q}$	
1	0	1	0	1	1	0	
0	1	0	1	0	0	1	
1	1	0	0				

1. Clock (T input) must be high.
2. The output state will not change when the input state goes from  $S_D = \bar{C}_D$  to  $S_D = C_D = 0$ . The output state cannot be predetermined in the case where the input goes from  $S_D = C_D = 1$  to  $S_D = C_D = 0$ .
3. Direct inputs ( $C_D$  and  $S_D$ ) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted  $t_n$  and the time period subsequent to this transition is denoted  $t_{n+1}$ .

MC9722P • MC9822P  
Dual J-K Flip-Flop



CLOCKED INPUT OPERATION ①

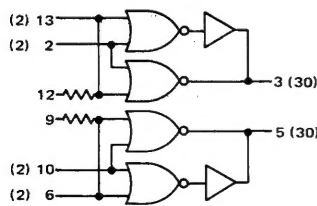
$t_n$ ②	$t_{n+1}$ ②	Q	$\bar{Q}$
S	C	Q	$\bar{Q}$
1	1	$Q_n$ ③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	$Q_n$ ③

$f_{Tog} = 4.0 \text{ MHz}$   
 $t_{pd} = 75 \text{ ns typ}$   
 $P_D = 24 \text{ mW typ}$  (Only Clock Input High)

1. Direct input ( $C_D$ ) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted  $t_n$  and the time period subsequent to this transition is denoted  $t_{n+1}$ .
3.  $Q_n$  is the state of the Q output in the time period  $t_n$ .

BUFFER

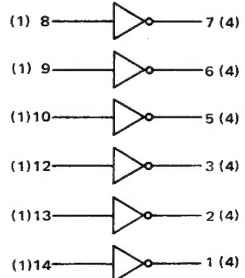
MC798P • MC898P  
Dual 2-Input Buffer



$3 = 2 + 13$   
 $t_{pd} = 57 \text{ ns}$   
 $P_D = 14 \text{ mW}$  (Input High)  
46 mW (Inputs Low)

INVERTER

MC9718P • MC9818P  
Hex Inverter

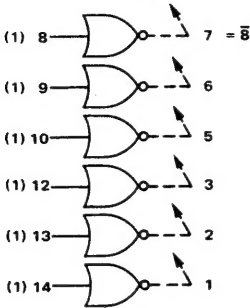


$7 = \bar{8}$   
 $t_{pd} = 27 \text{ ns}$   
 $P_D = 7.0 \text{ mW}$  (Input High)  
3.0 mW (Input Low)



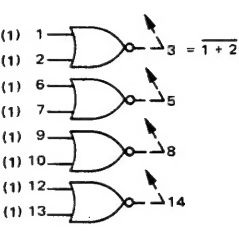
EXPANDERS

MC9720P • MC9820P  
Hex Expander



$t_{pd} = 12 \text{ ns}$   
 $P_D = 30 \text{ mW}$  (Inputs High)  
Negligible (Inputs Low)

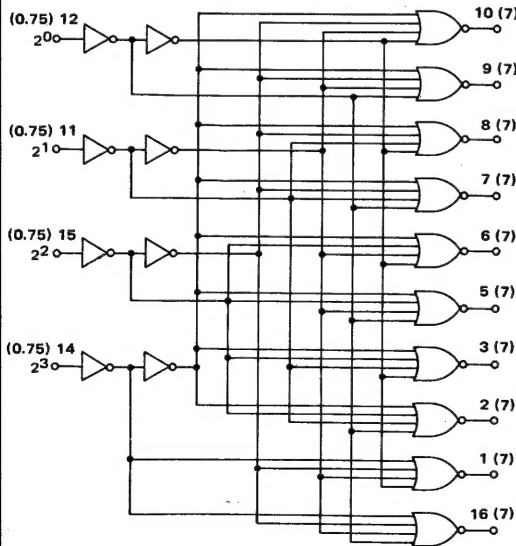
MC9721P • MC9821P  
Quad 2-Input Expander



$t_{pd} = 27 \text{ ns}$   
 $P_D = 20 \text{ mW typ}$  (Input High)  
Negligible (Inputs Low)

DECODER

MC770P • MC870P  
BCD-to-Decimal Decoder



INPUT (BCD)				OUTPUT (DECIMAL)									
2 <sup>3</sup>	2 <sup>2</sup>	2 <sup>1</sup>	2 <sup>0</sup>	0	1	2	3	4	5	6	7	8	9
14	15	11	12	10	9	8	7	6	5	3	2	1	16
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	1	0	0	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	0	0	1	0	0	0
0	1	1	0	0	0	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	0	0	0	0	1	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0	0	0

$t_{pd} = 36 \text{ ns}$   
 $P_D = 100 \text{ mW typ}$  (All inputs high)

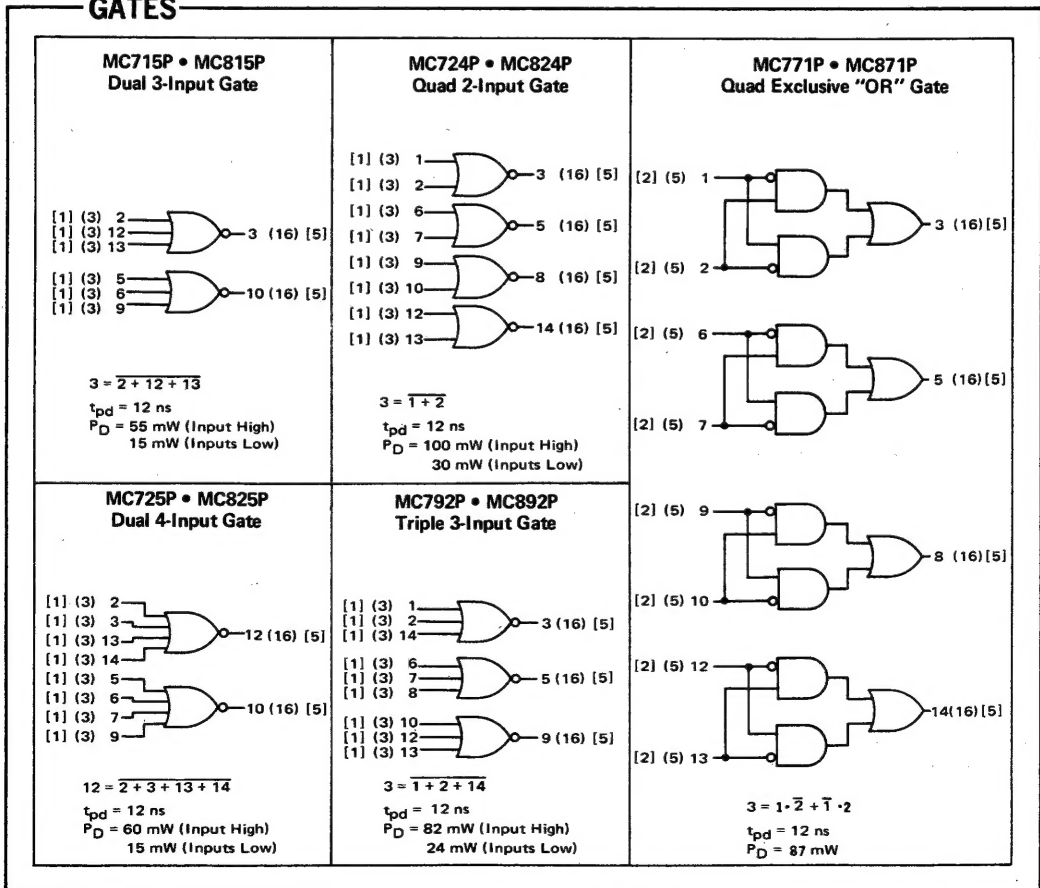
# MEDIUM-POWER MRTL DEVICES

The logic diagrams shown describe the MC700P/MC800P Series of medium-power resistor-transistor logic integrated circuits and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time ( $t_{pd}$ ), typical package power dissipation ( $P_D$ ), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis or brackets indicates the input loading factor (if on the circuit input terminal) or load driving ability — fan-out — (if on the circuit output terminal). The bracketed number is the loading factor when working with other medium-power devices; e.g., [1] is the MRTL load factor defined as 1 times the MRTL basic gate input current (600  $\mu$ Adc @ +25°C). The number

in parenthesis is the loading factor when working with mW MRTL devices; e.g., (3) is the MRTL load factor defined as 3 times the mW MRTL basic gate input current (140  $\mu$ Adc @ +25°C).

Using the parenthetic loading factors, these medium-power MRTL circuits are compatible with the low-power mW MRTL circuits shown in this section. The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. The loading data is valid over the temperature range of +15 to +55°C for the MC700P Series, and 0 to +75°C for the MC800P Series, with  $V_{CC} = 3.6 \text{ V} \pm 10\%$ .

## GATES



MEDIUM-POWER MRTL DEVICES (continued)

GATES (continued)

<p><b>MC9713P • MC9813P</b> Quad 2-Input AND Gate</p> <p><math>3 = 1 \cdot 2</math></p> <p>Avg <math>t_{pd} = 28</math> ns typ <math>P_D = 100</math> mW typ Operating <math>f = 14</math> MHz typ <math>* \text{Avg } t_{pd} = \frac{t_{on} + t_{off}}{2}</math></p>	<p><b>MC9714P • MC9814P</b> Quad 2-Input NAND Gate</p> <p><math>3 = 1 \cdot 2</math></p> <p><math>P_D = 145</math> mW typ Operating <math>f = 14</math> MHz typ</p>	<p><b>MC9715P • MC9815P</b> Quad 2-Input OR Gate</p> <p><math>3 = 1 + 2</math></p> <p><math>P_D = 100</math> mW typ (Inputs Low) <math>= 28</math> mW typ (Inputs High) Operating <math>f = 14</math> MHz typ</p>
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BUFFERS

<p><b>MC788P • MC888P Dual 3-Input Buffer</b> (Non-Inverting)</p> <p><math>14 = 1 + 2 + 3</math></p> <p><math>t_{pd} = 24</math> ns <math>P_D = 145</math> mW (Input High) <math>56</math> mW (Input Low) <math>12 = 1 + 2 + 3</math></p> <p>Outputs 12, 13, or 14 may not be used simultaneously. Outputs 8, 9, or 10 may not be used simultaneously.</p>	<p><b>MC799P • MC899P Dual Buffer</b></p> <p><math>10 = 5</math></p> <p><math>t_{pd} = 20</math> ns <math>P_D = 50</math> mW (Input High) <math>100</math> mW (Inputs Low)</p> <p>Outputs 2 and 3 may not be used simultaneously. Outputs 5 and 10 may not be used simultaneously.</p>
--	--

EXPANDERS

<p><b>MC785P • MC885P</b> Quad 2-Input Expander</p> <p><math>3 = 1 + 2</math></p> <p><math>t_{pd} = 12</math> ns <math>P_D = 20</math> mW (Input High) Negligible (Inputs Low)</p>	<p><b>MC786P • MC886P</b> Dual 4-Input Expander</p> <p><math>12 = 2 + 3 + 13 + 14</math></p> <p><math>t_{pd} = 12</math> ns <math>P_D = 20</math> mW (Input High) Negligible (Inputs Low)</p>	<p><b>MC9719P • MC9819P</b> Hex Expander</p> <p><math>7 = 8</math></p> <p><math>t_{pd} = 12</math> ns <math>P_D = 13</math> mW (Input High) Negligible (Inputs Low)</p>
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# FLIP-FLOPS

## DIRECT INPUT OPERATION ①

S <sub>D</sub>	C <sub>D</sub>	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

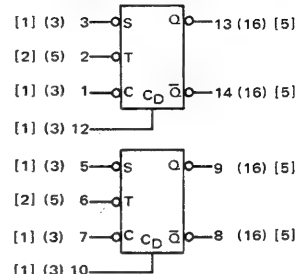
## CLOCKED INPUT OPERATION ③ all types

t <sub>n</sub> ④	t <sub>n+1</sub> ④	Q	$\bar{Q}$
S	C	Q	$\bar{Q}$
1	1	Q <sub>n</sub> ⑤	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q <sub>n</sub> ⑤

## J-K FLIP-FLOP TRUTH TABLES

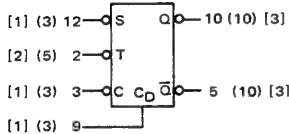
1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from S<sub>D</sub> =  $\bar{C}_D$  to S<sub>D</sub> = C<sub>D</sub> = 0. The output state cannot be predetermined in the case where the input goes from S<sub>D</sub> = C<sub>D</sub> = 1 to S<sub>D</sub> = C<sub>D</sub> = 0.
3. Direct inputs (C<sub>D</sub> and S<sub>D</sub>) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t<sub>n</sub> and the time period subsequent to this transition is denoted t<sub>n+1</sub>.
5. Q<sub>n</sub> is the state of the Q output in the time period t<sub>n</sub>.
6. Clock pulse fall time must be < 100 ns.

## MC791P • MC891P Dual J-K Flip-Flop



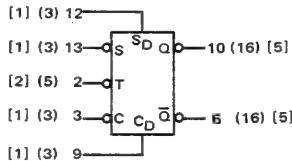
f<sub>Tog</sub> = 4 MHz  
P<sub>D</sub> = 190 mW (Only Clock Input High)  
160 mW (Inputs Low)

## MC723P • MC816P J-K Flip-Flop



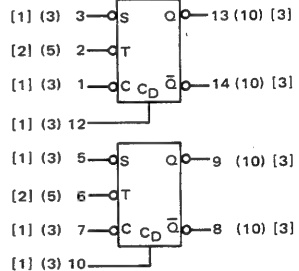
f<sub>Tog</sub> = 4 MHz  
P<sub>D</sub> = 91 mW (Only Clock Input High)  
79 mW (Inputs Low)

## MC726P • MC826P J-K Flip-Flop



f<sub>Tog</sub> = 4 MHz  
P<sub>D</sub> = 100 mW (Only Clock Input High)  
86 mW (Inputs Low)

## MC790P • MC890P Dual J-K Flip-Flop



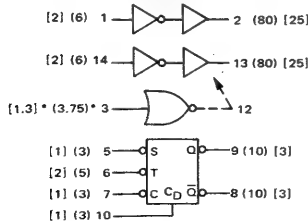
f<sub>Tog</sub> = 4 MHz  
P<sub>D</sub> = 182 mW (Only Clock Input High)  
158 mW (Inputs Low)

# MULTIFUNCTION DEVICES

## MC779P • MC879P

### Multifunction

(1 J-K FLIP-FLOP, 1 EXPANDER, 2 BUFFERS)



	f <sub>Tog</sub> MHz	t <sub>pd</sub> ns	P <sub>D</sub> mW
			(Input High) (Inputs Low)
FLIP-FLOP	4	—	91‡ 79
EACH BUFFER	—	15	25 45
EXPANDER	—	12	25 Negligible

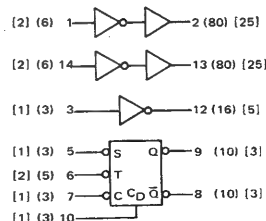
‡Only Clock Input High

\*Input loading factor is 3 for mW MRTL, or 1 for MRTL, if pin 12 is tied to pin 8 or 9 on the same package.

## MC787P • MC887P

### Multifunction

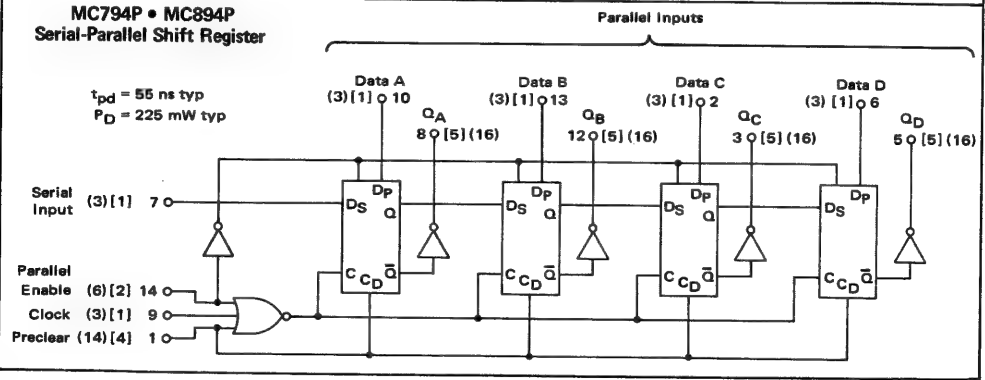
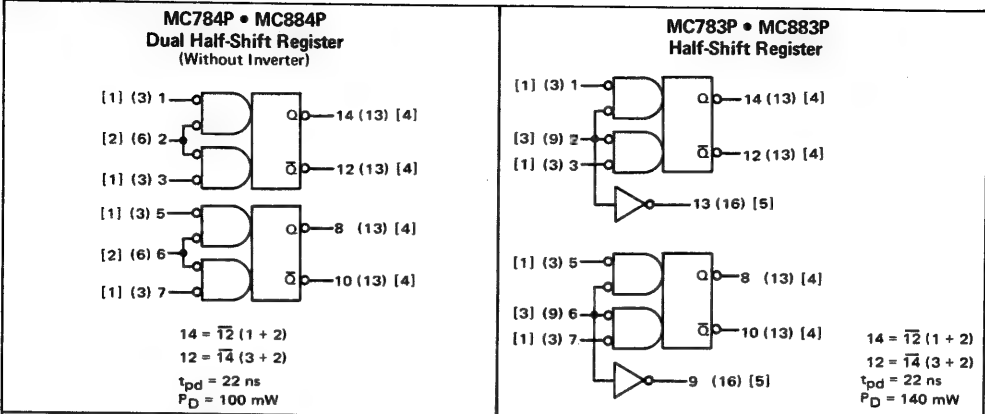
(1 J-K FLIP-FLOP, 1 INVERTER, 2 BUFFERS)



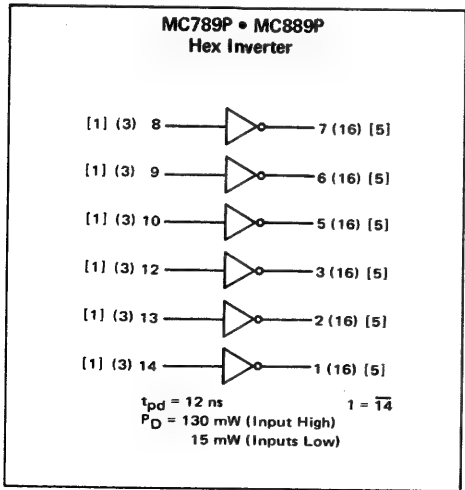
	f <sub>Tog</sub> MHz	t <sub>pd</sub> ns	P <sub>D</sub> mW
			(Input High) (Inputs Low)
FLIP-FLOP	4	—	91‡ 79
EACH BUFFER	—	15	25 45
INVERTER	—	12	22 8

‡Only Clock Input High

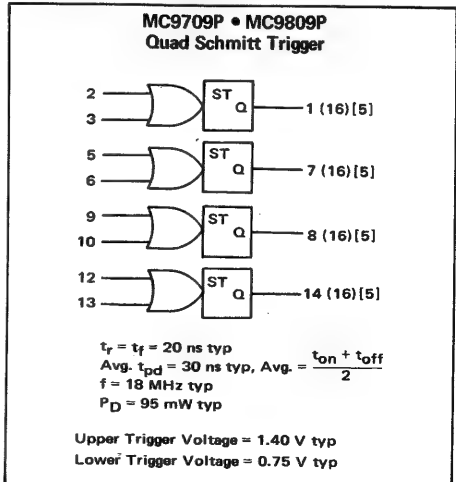
SHIFT REGISTERS



INVERTER

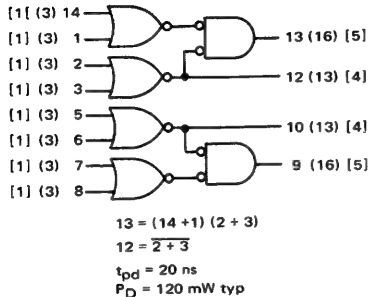


SCHMITT TRIGGER



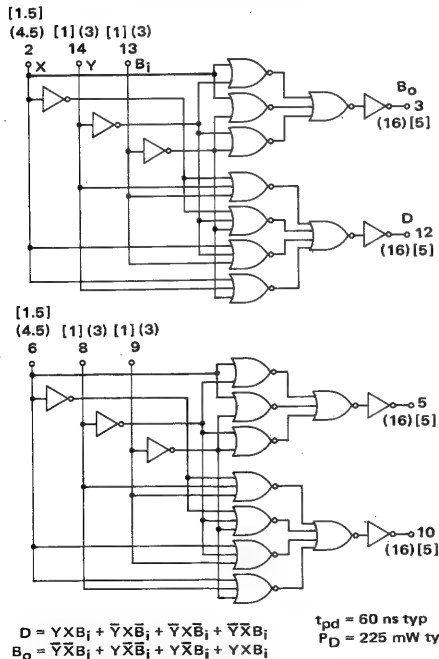
## HALF ADDER

### MC775P • MC875P Dual Half Adder



## FULL SUBTRACTOR

### MC797P • MC897P Dual Full Subtractor

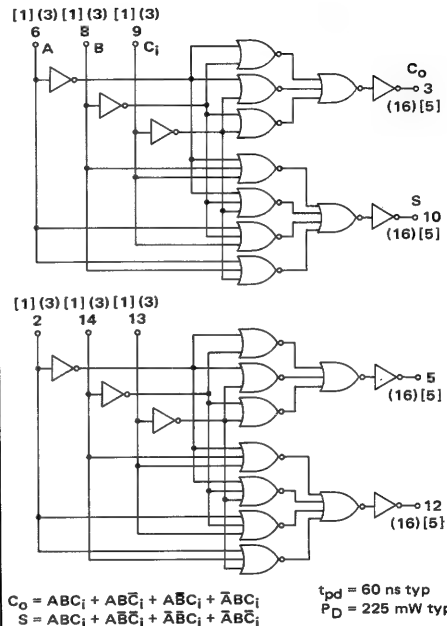


TRUTH TABLE

INPUT LOGIC LEVEL			OUTPUT LOGIC LEVEL	
X	Y	$B_i$	D	$B_o$
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

## FULL ADDERS

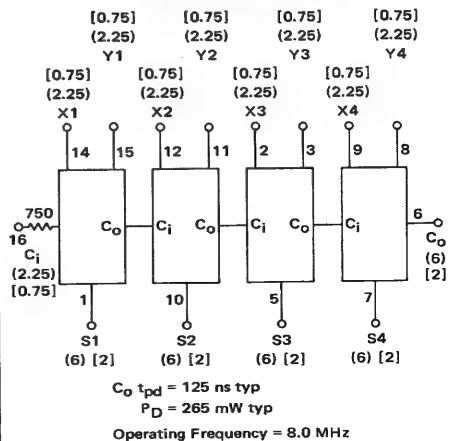
### MC796P • MC896P Dual Full Adder



TRUTH TABLE

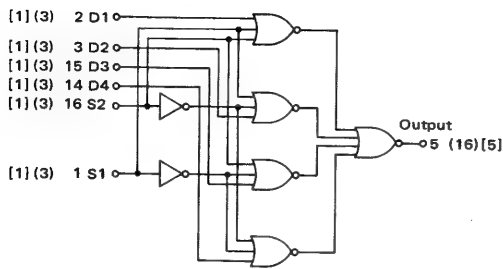
INPUT LOGIC LEVEL			OUTPUT LOGIC LEVEL	
A	B	$C_i$	S	$C_o$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

### MC9704P • MC9804P 4-Bit Parallel Full Adder



DATA ROUTING FUNCTIONS

MC9701P • MC9801P  
Dual 4-Channel Data Selector



TRUTH TABLE

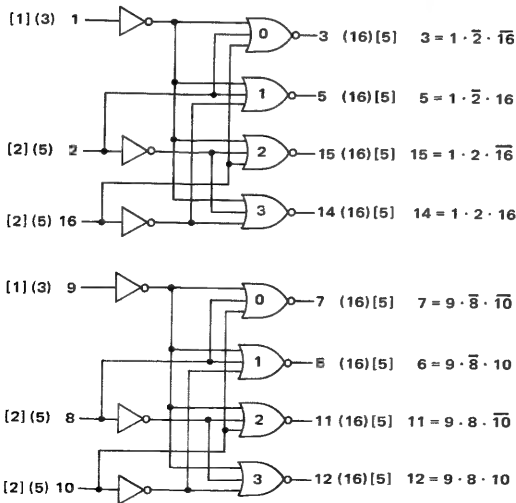
Input Select		Data Line Selected
S1	S2	
0	0	D1
0	1	D2
1	0	D3
1	1	D4

Output =  $\overline{S1} \overline{S2} D1 + \overline{S1} S2 D2 + S1 \overline{S2} D3 + S1 S2 D4$

Avg.  $t_{pd} = 25 \text{ ns typ}$       Avg.  $t_{pd} = \frac{t_{+} + t_{-}}{2}$   
 $P_D = 100 \text{ mW typ}$

Operating Frequency = 18 MHz typ  
(Both Selector Inputs and Data Inputs High)

MC9707P • MC9807P  
Dual 4-Channel Data Distributor



TRUTH TABLE

		INPUTS				OUTPUTS			
		D	S1	S2		0	1	2	3
Pin Numbers	Level	1	2	16	3	5	15	14	
	9	8	10	7	6	11	12		
	0	*	*	0	0	0	0	0	
	1	0	0	1	0	0	0	0	
1	0	1	0	1	0	0	0		
1	1	0	0	0	1	0	0		
1	1	1	0	0	0	1	0		

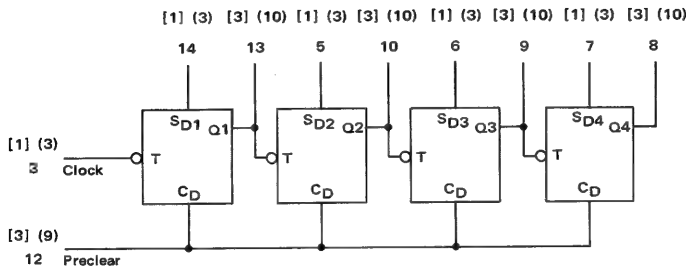
\* Either state.

Avg.  $t_{pd} = 25 \text{ ns typ}$   
 $P_D = 150 \text{ mW typ}$

\* Avg  $t_{pd} = \frac{t_{on} + t_{off}}{2}$

COUNTERS

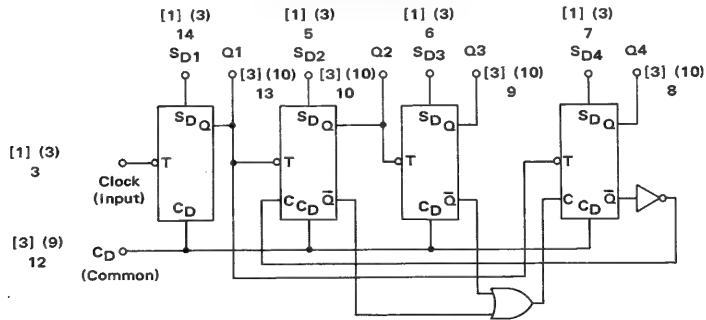
MC777P • MC877P  
Binary Up Counter



$f_{Tog} = 4.0 \text{ MHz}$   
 $P_D = 180 \text{ mW typ}$

DECODING LOGIC	
0	$\bar{A} \bar{B} \bar{C} \bar{D}$
1	$A \bar{B} \bar{C} \bar{D}$
2	$\bar{A} B \bar{C} \bar{D}$
3	$A B \bar{C} \bar{D}$
4	$\bar{A} \bar{B} C \bar{D}$
5	$A \bar{B} C \bar{D}$
6	$\bar{A} B C \bar{D}$
7	$A B C \bar{D}$
8	$\bar{A} \bar{B} C D$
9	$A \bar{B} C D$
10	$\bar{A} B C D$
11	$A B C D$
12	$\bar{A} \bar{B} C \bar{D}$
13	$A \bar{B} C \bar{D}$
14	$\bar{A} B C D$
15	$A B C D$

MC780P • MC880P  
Decade Up Counter



DECODING LOGIC

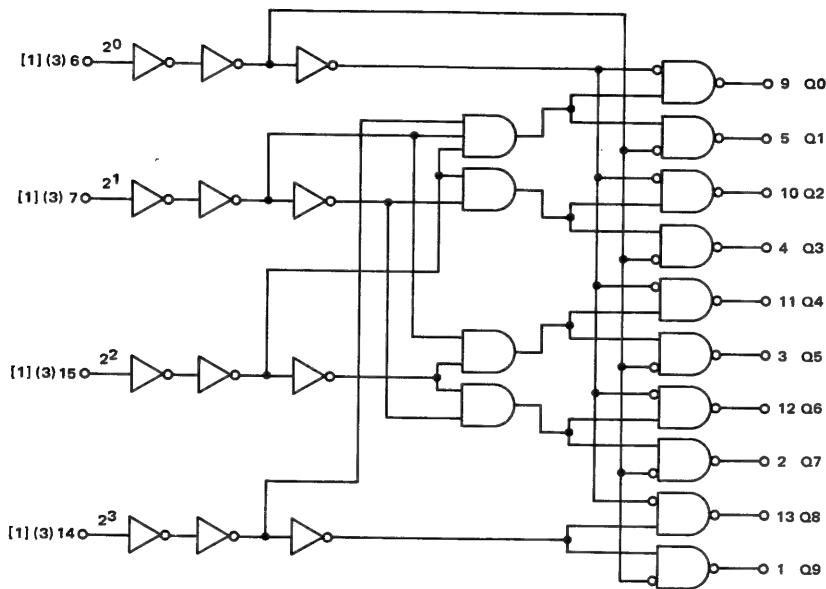
0	$\bar{A}$	$\bar{B}$	$\bar{C}$	$\bar{D}$
1	A	$\bar{B}$	$\bar{C}$	$\bar{D}$
2	$\bar{A}$	B	$\bar{C}$	$\bar{D}$
3	A	B	$\bar{C}$	$\bar{D}$
4	$\bar{A}$	$\bar{B}$	C	$\bar{D}$
5	A	$\bar{B}$	C	$\bar{D}$
6	$\bar{A}$	B	C	$\bar{D}$
7	A	B	C	$\bar{D}$
8	$\bar{A}$	$\bar{B}$	$\bar{C}$	D
9	A	$\bar{B}$	$\bar{C}$	D

$P_D = 250 \text{ mW typ}$   
 $f = 4.0 \text{ MHz}$   
Counting Frequency



DECODER/DRIVER

MC9760P • MC9860P  
BCD-to-Decimal Decoder/Driver



P<sub>D</sub> = 115 mW typ

TRUTH TABLE

Value Pin No. Logic Levels	INPUT* (BCD)				OUTPUT (DECIMAL)									
	2 <sup>0</sup>	2 <sup>1</sup>	2 <sup>2</sup>	2 <sup>3</sup>	0	1	2	3	4	5	6	7	8	9
6	7	15	14	9	5	10	4	11	3	12	2	13	1	
1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	0	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1	1
1	0	0	1	1	1	1	1	1	1	0	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	0	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	0	1	1
0	1	1	0	1	1	1	1	1	1	1	1	1	0	1

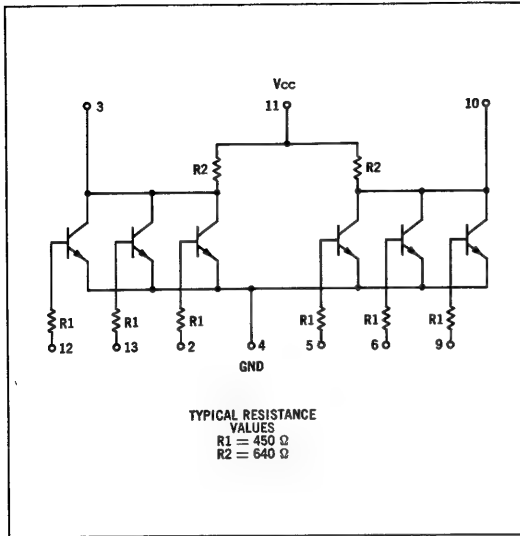
Logic "0" ≤ 1.5 Vdc @ 6.0 mA  
Logic "1" ≥ 65 Vdc (MC9760)  
Logic "1" ≥ 70 Vdc (MC9860)

\*Any input configuration not shown results in an indeterminate state at the outputs.

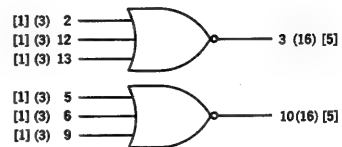
# DUAL 3-INPUT GATES

PLASTIC MRTL MC700P/800P series

## MC715P • MC815P



Two 3-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.



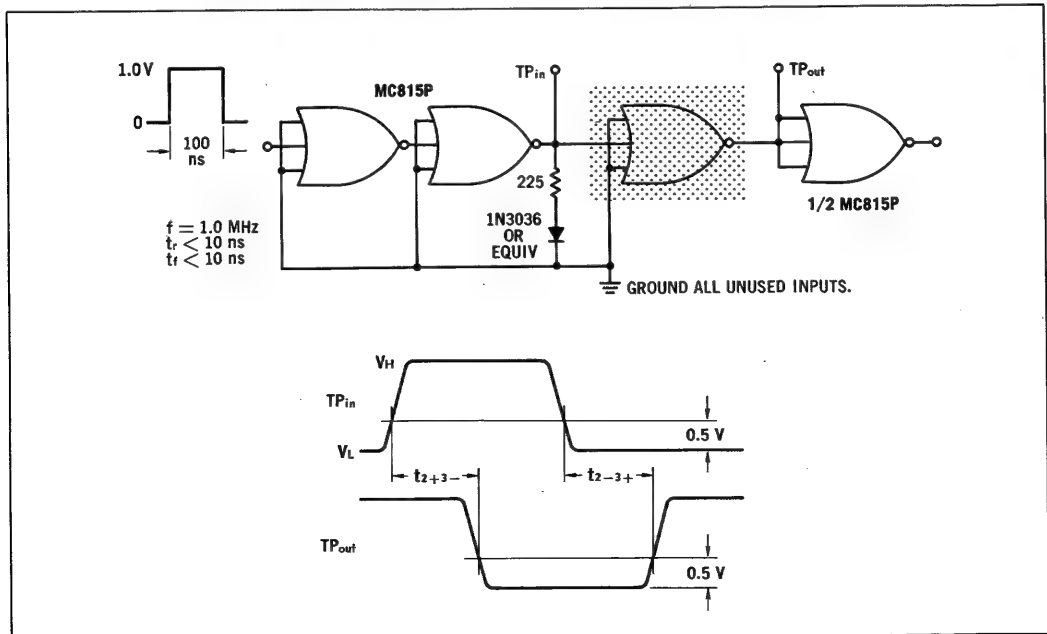
$$3 = 2 + 12 + 13$$

NUMBER IN PARENTHESES  
 INDICATES mW MRTL LOADING FACTOR

NUMBER IN BRACKETS  
 INDICATES MRTL LOADING FACTOR

$t_{pd} = 12 \text{ ns}$   
 $P_D = 55 \text{ mW (Input High)}$   
 $15 \text{ mW (Inputs Low)}$

## SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



## ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.  
The other gate is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC815P Test Limits							MC715P Test Limits							TEST VOLTAGE					Gnd		
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	APPLIED TO PINS LISTED BELOW:							
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		Min	Max	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>		V <sub>off</sub>	V <sub>CC</sub>
Input Current	I <sub>in</sub>	2 12 13	- - -	600 - ↓	- - -	600 - ↓	- - -	570 - ↓	μAdc - ↓	- - -	500 - ↓	- - -	500 - ↓	- - -	470 - ↓	μAdc - ↓	2 12 13	- - -	12, 13 2, 13 2, 12	- - -	11 - ↓	4 - ↓		
Output Current	I <sub>A5</sub>	3	3.00	-	3.00	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	3	-	2,12,13	11	4		
Output Voltage	V <sub>out</sub>	3 3 3	- - -	500 - ↓	- - -	400 - ↓	- - -	400 - ↓	mVdc - ↓	- - -	400 - ↓	- - -	300 - ↓	- - -	320 - ↓	mVdc - ↓	- - -	12 13 2	- - -	- - -	11 - ↓	2,4,13 2,4,12 4,12,13		
Saturation Voltage	V <sub>CE(sat)</sub>	3 3 3	- - -	400 - ↓	- - -	300 - ↓	- - -	350 - ↓	mVdc - ↓	- - -	300 - ↓	- - -	290 - ↓	- - -	320 - ↓	mVdc - ↓	- - -	- - -	12 13 2	- - -	11 - ↓	2,4,13 2,4,12 4,12,13		
Switching Time	t <sub>on</sub> + t <sub>off</sub>	3, 13	-	-	-	48	-	-	ns	-	-	-	48	-	-	ns	Pulse In 13	Pulse Out 3	-	-	11	2,4,12		

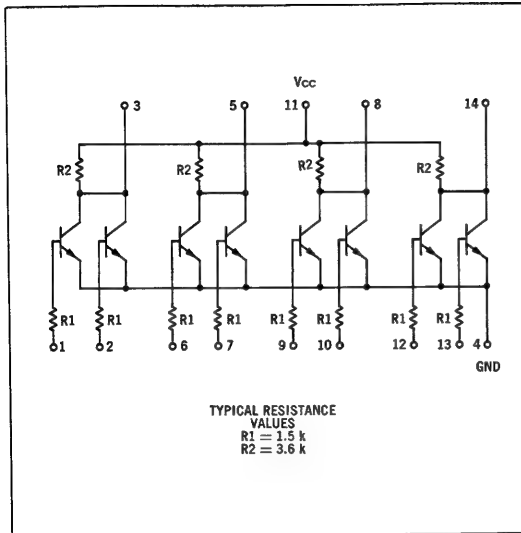
Ground input pins of gate not under test. Other pins not listed are left open.

@ Test Temperature  
 MC815P { 0°C  
 +25°C  
 +75°C  
 MC715P { +15°C  
 +25°C  
 +55°C

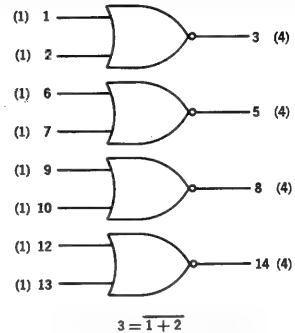
# QUAD 2-INPUT GATES

PLASTIC mW MRTL MC700P/800P series

## MC717P • MC817P



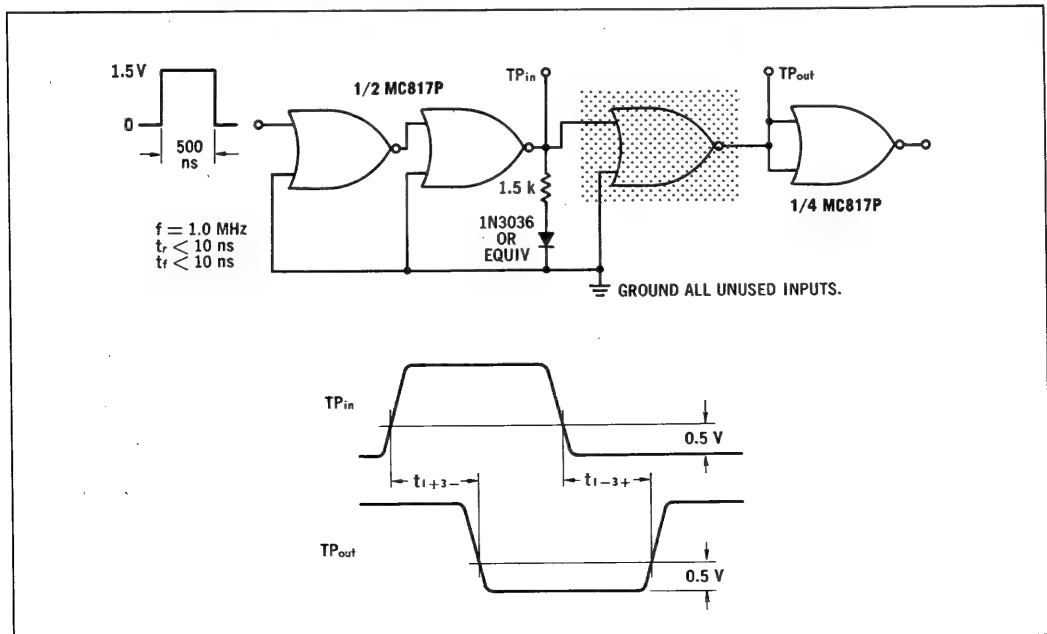
Four 2-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.



NUMBER IN PARENTHESES INDICATES LOADING FACTOR

$t_{pd} = 27\text{ ns}$   
 $P_D = 20\text{ mW}$  (Input High)  
 $5.0\text{ mW}$  (Inputs Low)

## SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



## ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.  
The other gates are tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC817P Test Limits							MC717P Test Limits							TEST VOLTAGE					Gnd
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	APPLIED TO PINS LISTED BELOW:					
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		V <sub>in</sub>	V <sub>on</sub>	V <sub>bot</sub>	V <sub>off</sub>	V <sub>cc</sub>	
Input Current	I <sub>in</sub>	1 2	- 150	- 150	- 140	- 140	- 140	μA <sub>dc</sub> μA <sub>dc</sub>	- -	150 150	- -	150 150	- -	150 150	μA <sub>dc</sub> μA <sub>dc</sub>	1 2	- -	2 1	- -	11 11	4 4	
Output Current	I <sub>A4</sub>	3	570	-	570	-	535	-	μA <sub>dc</sub>	570	-	570	-	570	-	μA <sub>dc</sub>	-	3	-	1, 2	11	4
Output Voltage	V <sub>out</sub>	3 3	- 400	- 400	- 350	- 350	- 300	mV <sub>dc</sub> mV <sub>dc</sub>	- -	400 400	- -	300 300	- -	320 320	mV <sub>dc</sub> mV <sub>dc</sub>	- -	1 2	- -	- -	11 11	2, 4 1, 4	
Saturation Voltage	V <sub>CE(sat)</sub>	3 3	- 250	- 250	- 250	- 250	- 250	mV <sub>dc</sub> mV <sub>dc</sub>	- -	220 220	- -	230 230	- -	320 320	mV <sub>dc</sub> mV <sub>dc</sub>	- -	- -	1 2	- -	11 11	2, 4 1, 4	
Switching Time	t <sub>on</sub> + t <sub>off</sub>	1, 3	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	Pulse In 1	Pulse Out 3	-	-	11	2, 4

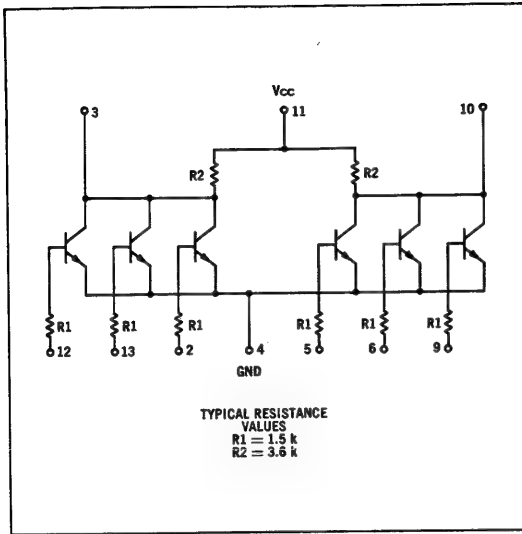
Ground input pins of gates not under test. Other pins not listed are left open.

TEST VOLTAGE VALUES					
(Volts)					
@ Test Temperature	V <sub>in</sub>	V <sub>on</sub>	V <sub>DOT</sub>	V <sub>off</sub>	V <sub>cc</sub>
MC817P { 0°C	0.880	0.850	1.80	0.500	3.60
+25°C	0.830	0.800	1.80	0.460	3.60
+75°C	0.740	0.710	1.80	0.400	3.60
MC717P { +15°C	0.865	0.865	1.80	0.475	3.60
+25°C	0.850	0.850	1.80	0.460	3.60
+55°C	0.800	0.800	1.80	0.430	3.60

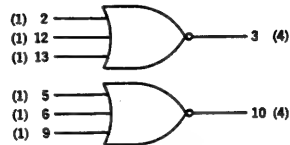
# DUAL 3-INPUT GATES

PLASTIC mW MRTL MC700P/800P series

## MC718P • MC818P



Two 3-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.

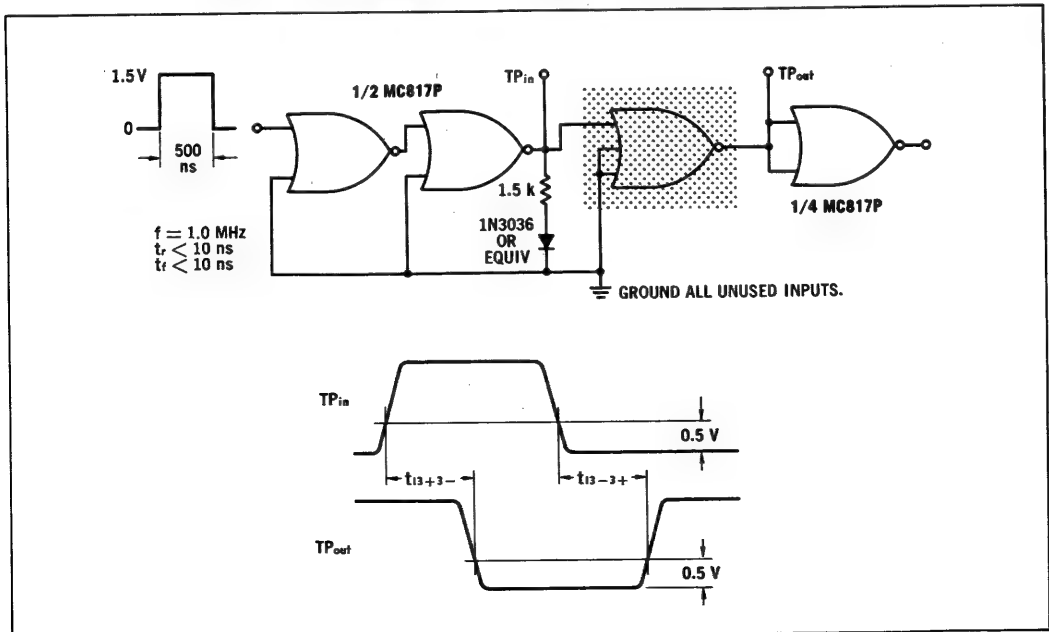


$$3 = 2 + 12 + 13$$

NUMBER IN PARENTHESES INDICATES LOADING FACTOR

$t_{pd} = 27 \text{ ns}$   
 $P_D = 12 \text{ mW (Input High)}$   
 $2.5 \text{ mW (Inputs Low)}$

## SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



## ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.  
The other gate is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC818P Test Limits							MC718P Test Limits							TEST VOLTAGE					Gnd
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	APPLIED TO PINS LISTED BELOW:					
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	
			0°C		+25°C		+75°C			+15°C		+25°C		+55°C			V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	
Input Current	I <sub>in</sub>	2 12 13	- ↓ -	150 ↓ -	- ↓ -	140 ↓ -	- ↓ -	140 ↓ -	μA <sub>dc</sub> ↓ ↓	- ↓ -	150 ↓ -	- ↓ -	150 ↓ -	- ↓ -	150 ↓ ↓	μA <sub>dc</sub> ↓ ↓	2 12 13	- - -	12, 13 2, 13 2, 12	- - -	11 ↓ ↓	4 ↓ ↓
Output Current	I <sub>A4</sub>	3	570	-	570	-	535	-	μA <sub>dc</sub>	570	-	570	-	570	-	μA <sub>dc</sub>	3	-	-	2, 12, 13	11	4
Output Voltage	V <sub>out</sub>	3 3 3	- ↓ -	400 ↓ -	- ↓ -	350 ↓ -	- ↓ -	300 ↓ -	mV <sub>dc</sub> ↓ ↓	- ↓ -	400 ↓ -	- ↓ -	300 ↓ -	- ↓ -	320 ↓ ↓	mV <sub>dc</sub> ↓ ↓	- - -	12 13 2	- - -	- - -	11 ↓ ↓	2, 4, 13 2, 4, 13 4, 12, 13
Saturation Voltage	V <sub>CE(sat)</sub>	3 3 3	- ↓ -	250 ↓ -	- ↓ -	250 ↓ -	- ↓ -	250 ↓ ↓	mV <sub>dc</sub> ↓ ↓	- ↓ -	220 ↓ -	- ↓ -	230 ↓ ↓	- ↓ -	320 ↓ ↓	mV <sub>dc</sub> ↓ ↓	- - -	- - -	12 13 2	- - -	11 ↓ ↓	2, 4, 13 2, 4, 12 4, 12, 13
Switching Time	t <sub>on</sub> + t <sub>off</sub>	3, 13	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	Pulse In	Pulse Out	-	-	11	2, 4, 12
																	13	3				

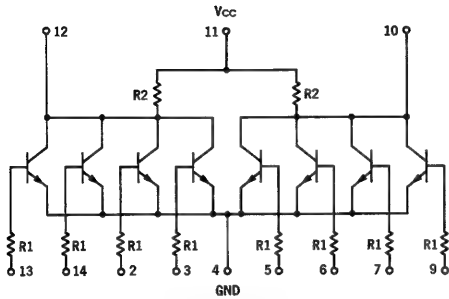
Ground unused input pins. Other pins not listed are left open.

	@ Test Temperature	TEST VOLTAGE VALUES				
		(Volts)				
MC818P	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60
MC718P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

# DUAL 4-INPUT GATES

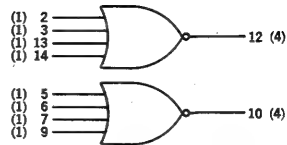
PLASTIC mW MRTL MC700P/800P series

## MC719P • MC819P



TYPICAL RESISTANCE  
VALUES  
R1 = 1.5 k  
R2 = 3.6 k

Two 4-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.

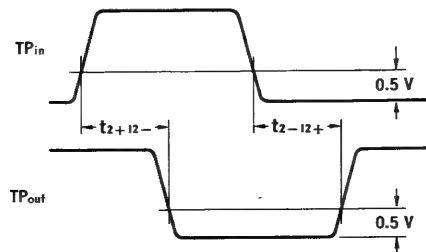
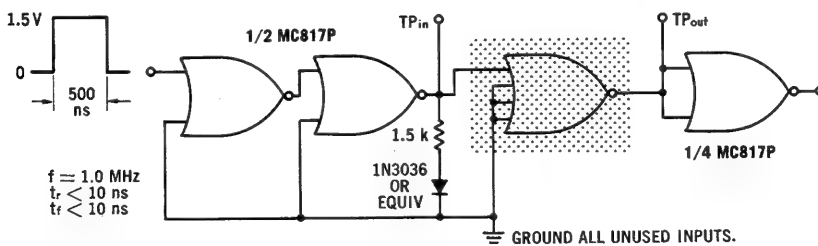


$$12 = 2 + 3 + 13 + 14$$

NUMBER IN PARENTHESES  
INDICATES LOADING FACTOR

$t_{pd} = 27 \text{ ns}$   
 $P_D = 13 \text{ mW (Input High)}$   
 $2.5 \text{ mW (Inputs Low)}$

## SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





## ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.  
The other gate is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC819P Test Limits							MC719P Test Limits							TEST VOLTAGE						Gnd
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	APPLIED TO PINS LISTED BELOW:						
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>		
Input Current	I <sub>in</sub>	2	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	2	-	3,13,14	-	11	4	
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	2,13,14	-	↓	↓	
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	13	-	2,3,14	-	↓	↓	
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	14	-	2,3,13	-	↓	↓	
Output Current	I <sub>A4</sub>	12	570	-	570	-	535	-	μAdc	570	-	570	-	570	-	μAdc	-	12	-	2,3,13,14	11	4	
Output Voltage	V <sub>out</sub>	12	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-	11	2,3,4,14	
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	14	-	-	↓	2,3,4,13	
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2	-	-	↓	3,4,13,14	
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	2,4,13,14	
Saturation Voltage	V <sub>CE(sat)</sub>	12	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	13	-	11	2,3,4,14	
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	14	-	↓	2,3,4,13	
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2	-	-	↓	3,4,13,14	
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	2,4,13,14	
Switching Time	t <sub>on</sub> + t <sub>off</sub>	2, 12	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	Pulse In	Pulse Out	-	-	11	3,4,13,14	
			-	-	-	-	-	-	-	-	2	12	-	-	-	-	-	-					

Ground inputs of gate not under test. Other pins not listed are left open.

@ Test Temperature  
 MC819P { 0°C  
 +25°C  
 +75°C  
 MC719P { +15°C  
 +25°C  
 +55°C

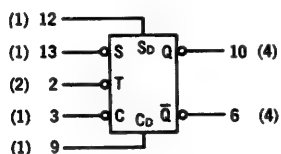
TEST VOLTAGE VALUES					
(Volts)					
V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	
0.880	0.850	1.80	0.500	3.60	
0.830	0.800	1.80	0.460	3.60	
0.740	0.710	1.80	0.400	3.60	
0.865	0.865	1.80	0.475	3.60	
0.850	0.850	1.80	0.460	3.60	
0.800	0.800	1.80	0.430	3.60	

# J-K FLIP-FLOPS

PLASTIC mW MRTL MC700P/800P series

## MC722P • MC822P

J-K flip-flop with direct clear and direct set inputs in addition to the clocked inputs.



NUMBER IN PARENTHESES INDICATES LOADING FACTOR

$f_{\text{op}} = 1.0 \text{ MHz}$   
 $P_D = 24 \text{ mW}$  (Only Clock Input High)  
20 mW (Inputs Low)

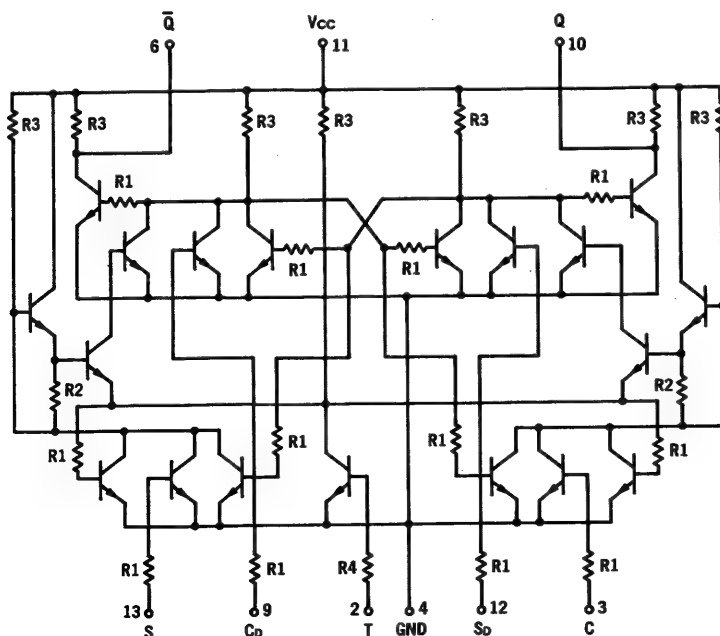
### DIRECT INPUT OPERATION ①

$S_0$	$C_0$	Q	$\bar{Q}$
0	0	②	③
1	0	1	0
0	1	0	1
1	1	0	0

### CLOCKED INPUT OPERATION ②

$t_n$	$t_{n+1}$	Q	$\bar{Q}$
S	C	$Q_n$	$\bar{Q}_n$
1	1	0	1
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	$Q_n$

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from  $S_0 = \bar{C}_0$  to  $S_0 = C_0 = 0$ . The output state cannot be predetermined in the case where the input goes from  $S_0 = C_0 = 1$  to  $S_0 = C_0 = 0$ .
3. Direct inputs ( $S_0$  and  $C_0$ ) must be low.
  - 0 = low state
  - 1 = high state
  - $t_n$  = time period prior to negative transition of clock pulse
  - $t_{n+1}$  = time period subsequent to negative transition of clock pulse
  - $Q_n$  = state of Q output in time period  $t_n$



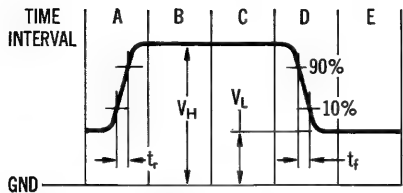
TYPICAL RESISTANCE VALUES  
R1 = 1.5 k    R3 = 3.6 k  
R2 = 2.0 k    R4 = 750  $\Omega$

# ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC822P Test Limits							MC722P Test Limits							TEST VOLTAGE					Gnd	
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	APPLIED TO PINS LISTED BELOW:						
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>		
Input Current	2I <sub>in</sub> I <sub>in</sub>	2	-	300	-	280	-	280	μAdc	-	300	-	300	-	300	μAdc	2	-	3, 13	-	11	4	
		3	-	150	-	140	-	140		-	150	-	150	-	150		3	-	12	-			
		9	-		-		-			-		-		-			9	-		-			
		12	-		-		-			-		-		-			12	-		-			
		13	-	↓		↓		↓	↓		↓		↓		↓	↓		13	-	9	-	↓	↓
Output Current	I <sub>A4</sub>	6	570	-	570	-	535	-	μAdc	570	-	570	-	570	-	μAdc	6	9	12	-	11	4	
		10	570	-	570	-	535	-	μAdc	570	-	570	-	570	-	μAdc	10	12	9	-	11	4	
Saturation Voltage	V <sub>CE(sat)</sub>	6	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	12	-	-	9	11	4
		6*#	-		-		-			-		-		-			-	13	-	-	3		
		6*##	-		-		-			-		-		-			-	-	-	3, 13			
		10	-		-		-			-		-		-			-	3, 13	-	-	-		
		10*##	-		-		-			-		-		-			-	9	-	12			
		10*#	-		-		-			-		-		-			-	3	-	13			
		10*##	-	↓		↓		↓	↓		↓		↓		↓	↓		-	3, 13	-	-	3, 13	↓

Pins not listed are left open.  
 \* = Clock Pulse to pin 2, see Figure 1.  
 # = Pin 9 HIGH } Set by a momentary application of V<sub>BOT</sub> prior to the application of the negative-going clock pulse.  
 ## = Pin 12 HIGH }

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

- A. Voltage applied to Clock pin is raised to  $V_H$ .  $t_r$  is not critical but should be  $< 1.0 \mu s$ .
- B. Biases of all other inputs are applied.  $V_{CC}$  is applied without interruption throughout the testing.
- C. Apply momentary ground (when applicable).
- D. Clock pulse is allowed to fall to  $V_L$ .  $t_f$  must remain within 10 ns minimum and 200 ns maximum.
- E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

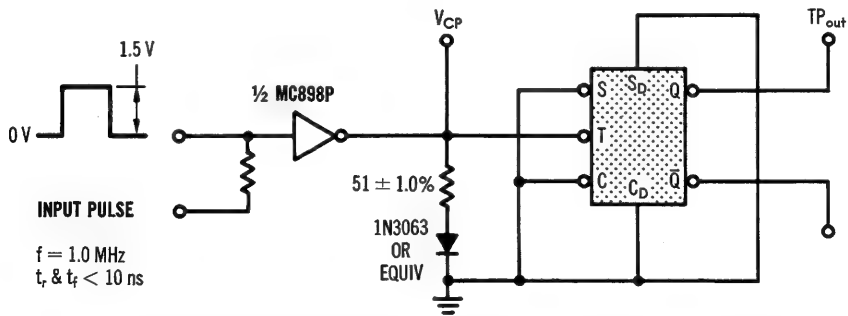
MC822P

$T_A$	$V_L$	$V_H$
+ 25°C	+ 0.460 V $\pm$ 2.0 mV	+ 0.850 V $\pm$ 2.0 mV
0°C	+ 0.500 V $\pm$ 2.0 mV	+ 0.900 V $\pm$ 2.0 mV
+ 75°C	+ 0.400 V $\pm$ 2.0 mV	+ 0.760 V $\pm$ 2.0 mV

MC722P

$T_A$	$V_L$	$V_H$
+ 25°C	+ 0.460 V $\pm$ 2.0 mV	+ 0.900 V $\pm$ 2.0 mV
+ 15°C	+ 0.475 V $\pm$ 2.0 mV	+ 0.915 V $\pm$ 2.0 mV
+ 55°C	+ 0.430 V $\pm$ 2.0 mV	+ 0.850 V $\pm$ 2.0 mV

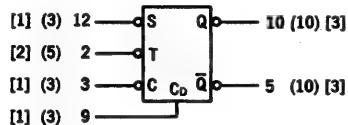
FIGURE 2 — TOGGLE MODE TEST CIRCUIT



THE SENSE FREQUENCY AT  $TP_{out}$  (0.5 MHz) SHOULD BE  $\frac{1}{2}$  THE FREQUENCY AT  $V_{CP}$  WHEN THE DUTY CYCLE IS VARIED BETWEEN 25% AND 75%.

**MC723P • MC816P**

J-K flip-flop with a direct clear input in addition to the clocked inputs.



$f_{reg} = 4 \text{ MHz}$

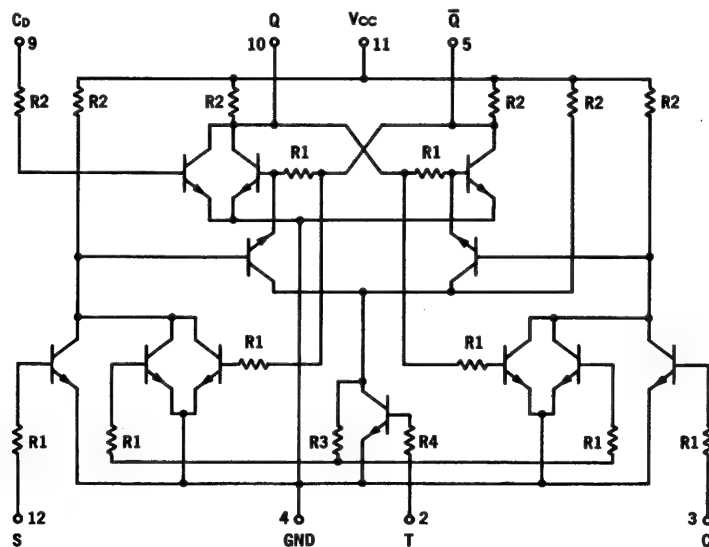
$P_D = 91 \text{ mW}$  (Only Clock Input High)  
 $79 \text{ mW}$  (Inputs Low)

**CLOCKED INPUT OPERATION ①**

$t_n$ ③		$t_{n+1}$ ④	
S	C	Q	$\bar{Q}$
1	1	$Q_n$ ⑤	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	$Q_n$ ⑤

1. Direct input ( $C_D$ ) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted  $t_n$  and the time period subsequent to this transition is denoted  $t_{n+1}$ .
3.  $Q_n$  is the state of the Q output in the time period  $t_n$ .
4. Clock pulse fall time must be  $< 100 \text{ ns}$ .

NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL  
 NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL



**TYPICAL RESISTANCE VALUES**

$R1 = 450 \Omega$   
 $R2 = 640 \Omega$   
 $R3 = 510 \Omega$   
 $R4 = 225 \Omega$

## ELECTRICAL CHARACTERISTICS

																	TEST VOLTAGE VALUES				
																	(Volts)				
																	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>cc</sub>
																	0.960	0.930	1.80	0.570	3.60
																	0.910	0.880	1.80	0.500	3.60
																	0.820	0.790	1.80	0.450	3.60
																	0.865	0.865	1.80	0.475	3.60
																	0.850	0.850	1.80	0.460	3.60
																	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC816P Test Limits							MC723P Test Limits							TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					Gnd
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>cc</sub>	
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max							
Input Current	2I <sub>in</sub> I <sub>in</sub>	2	-	1200	-	1200	-	1140	μAdc	-	1000	-	1000	-	940	μAdc	2	-	3, 12	-	11	4
		3	-	600	-	600	-	570		-		-		-			3	-	10	-		
		9	-		-		-			-		-		-			9	-	5	-		
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	12	-	5	-	↓	↓
Output Current	I <sub>A3</sub>	5	1.80	-	1.80	-	1.71	-	mAdc	1.65	-	1.65	-	1.56	-	mAdc	-	5	9, 12	-	11	4
		5	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	5, 9	12	-	↓	4
		10		-		-		-	↓		-		-		-	↓	-	10	3	9	↓	4, 5 §
Output Voltage	V <sub>out</sub>	10	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	9	-	-	11	4, 5
		10*##	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3, 12	-	-	↓	4, 9
		10*	-		-		-		↓	-		-		-		↓	-	-	-	12	↓	
		10*##	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	3, 12	3, 12	↓	↓
Saturation Voltage	V <sub>CE(sat)</sub>	5	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	-	9	11	4, 5
		10	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	9	-	↓	4, 5
		10	-		-		-		↓	-		-		-		↓	-	-	-	-	↓	4, 10 §
Turn-On Voltage	V <sub>on</sub>	10*##Δ	930	-	880	-	790	-	mVdc	865	-	850	-	800	-	mVdc	-	3, 12	-	-	11	4, 9
		10*Δ	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	-	-	3	↓	↓
		10*#Δ	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	-	3, 12	3, 12	↓	↓

Pins not listed are left open.

# = Pin 10 LOW } Set by a momentary ground prior to the application  
 ## = Pin 5 LOW } of the negative-going Clock pulse.

§ = Silicon diode to ground.

\* = Clock Pulse to pin 2, See Figure 1.

Δ = MC816P pin 10 loaded by: 1.56 mAdc (0°C and +75°C)

1.65 mAdc (+25°C)

MC723P pin 10 loaded by: 1.56 mAdc (+15°C and +55°C)

1.65 mAdc (+25°C)

FIGURE 1 — CLOCK PULSE DEFINITION

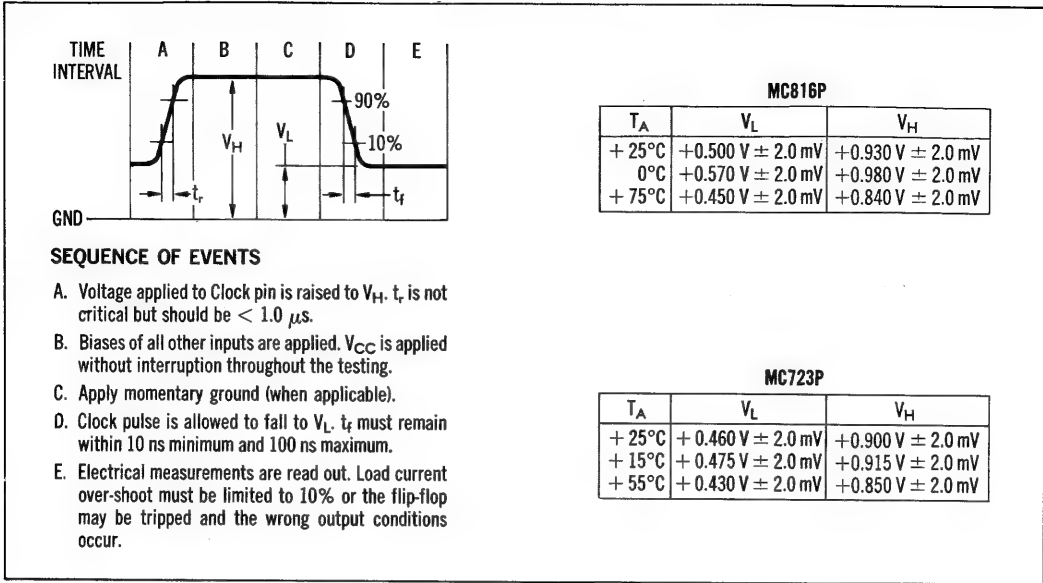
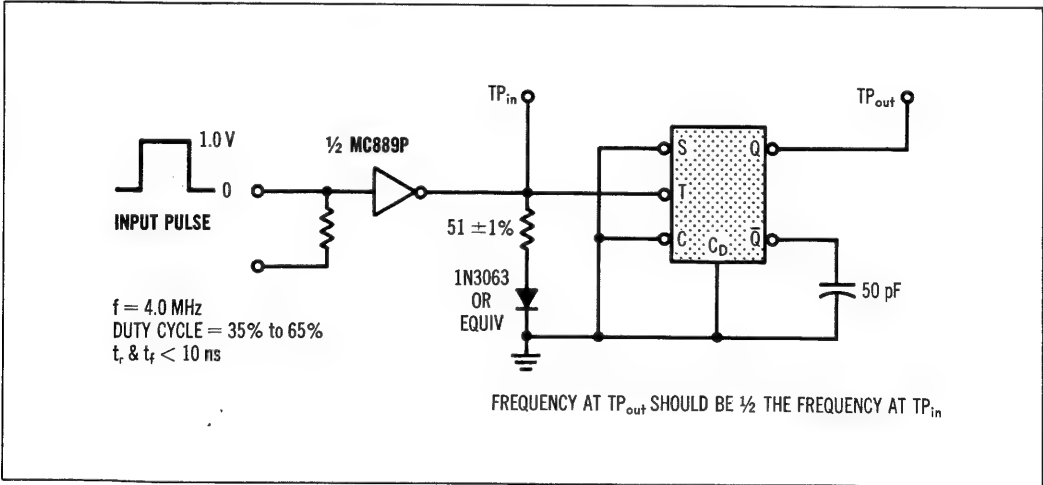
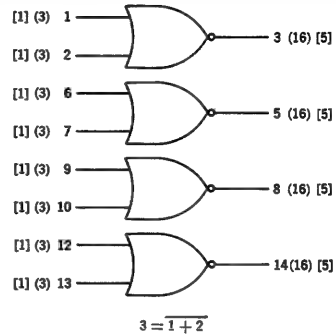


FIGURE 2 — TOGGLE MODE TEST CIRCUIT



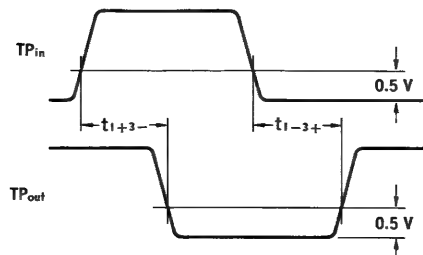
## PLASTIC MRTL MC700P/800P series

Four 2-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.



$t_{pd} = 12 \text{ ns}$   
 $P_D = 100 \text{ mW (Input High)}$   
 $30 \text{ mW (Inputs Low)}$

The diagram shows a square wave input signal with a period of 100 ns and a frequency of 1.0 MHz. The input signal is connected to the MC815P. The output signal is shown as a square wave with a period of 100 ns and a frequency of 1.0 MHz. The output signal is labeled TP<sub>in</sub> and TP<sub>out</sub>. The output signal is connected to a 225 ohm resistor and a 1N3036 diode. The output signal is also connected to a shaded area labeled 1/2 MC815P. The output signal is connected to a shaded area labeled 1/2 MC815P. The output signal is connected to a shaded area labeled 1/2 MC815P.





## ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.  
The other gates are tested in the same manner.

Test Limits				TEST VOLTAGE						Gnd
				APPLIED TO PINS LISTED BELOW:						
				(Volts)						
				V <sub>IN</sub>	V <sub>ON</sub>	V <sub>BOT</sub>	V <sub>OFF</sub>	V <sub>CC</sub>		
+55°C										
Min	Max	Unit								
-	470	μAdc	1	-	2	-	11	4		
-	470	μAdc	2	-	1	-	11	4		
2.50	-	mAdc	-	3	-	1, 2	11	4		
-	320	mVdc	-	1	-	-	11	2, 4		
-	320	mVdc	-	2	-	-	11	1, 4		
-	320	mVdc	-	-	1	-	11	2, 4		
-	320	mVdc	-	-	2	-	11	1, 4		
			Pulse In	Pulse Out						
-	-	ns	1	3	-	-	11	2, 4		

Characteristic	Symbol	Pin Under Test	MC824P Test Limits							MC724P Test Limits							TEST VOLTAGE APPLIED TO PINS LISTED BELOW:						Gnd
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	V <sub>in</sub>	V <sub>on</sub>	V <sub>Bot</sub>	V <sub>off</sub>	V <sub>CC</sub>		
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max								
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max								
Input Current	I <sub>in</sub>	1 2	- -	600 600	- -	600 600	- -	570 570	μA <sub>dc</sub> μA <sub>dc</sub>	- -	500 500	- -	500 500	- -	470 470	μA <sub>dc</sub> μA <sub>dc</sub>	1 2	- -	2 1	- -	11 11	4 4	
Output Current	I <sub>A5</sub>	3	3.0	-	3.0	-	2.85	-	mA <sub>dc</sub>	2.65	-	2.65	-	2.50	-	mA <sub>dc</sub>	-	3	-	1,2	11	4	
Output Voltage	V <sub>out</sub>	3 3	- -	500 500	- -	400 400	- -	400 400	mV <sub>dc</sub> mV <sub>dc</sub>	- -	400 400	- -	300 300	- -	320 320	mV <sub>dc</sub> mV <sub>dc</sub>	- -	1 2	- -	- -	11 11	2,4 1,4	
Saturation Voltage	V <sub>CE(sat)</sub>	3 3	- -	400 400	- -	300 300	- -	350 350	mV <sub>dc</sub> mV <sub>dc</sub>	- -	300 300	- -	290 290	- -	320 320	mV <sub>dc</sub> mV <sub>dc</sub>	- -	- -	1 2	- -	11 11	2,4 1,4	
Switching Time	t <sub>on</sub> + t <sub>off</sub>	1, 3	-	-	-	48	-	-	ns	-	-	-	48	-	-	ns	Pulse In 1	Pulse Out 3	-	-	11	2, 4	

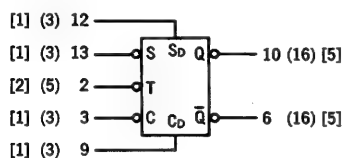
Ground input pins of gates not under test. Other pins not listed are left open.





**MC726P • MC826P**

J-K flip-flop with direct clear and direct set inputs in addition to the clocked inputs.



$f_{\text{reg}} = 4 \text{ MHz}$

$P_D = 100 \text{ mW}$  (Only Clock Input High)  
 $86 \text{ mW}$  (Inputs Low)

**CLOCKED INPUT OPERATION ①**

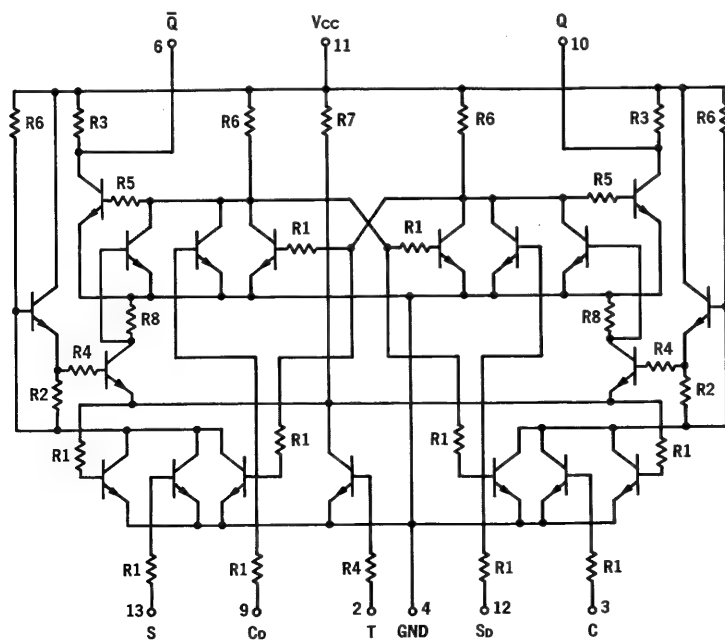
$t_n$ ②		$t_{n+1}$ ③	
S	C	Q	$\bar{Q}$
1	1	$Q_n$ ④	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	$Q_n$ ④

**DIRECT INPUT OPERATION ④**

$S_D$	$C_D$	Q	$\bar{Q}$
0	0	⑤	⑤
1	0	1	0
0	1	0	1
1	1	0	0

1. Direct inputs ( $C_D$  and  $S_D$ ) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted  $t_n$  and the time period subsequent to this transition is denoted  $t_{n+1}$ .
3.  $Q_n$  is the state of the Q output in the time period  $t_n$ .
4. Clock (T) to remain unchanged.
5. The output state will not change when the input state goes from  $S_D = C_D$  to  $S_D = C_D = 0$ . The output state cannot be predetermined in the case where the input goes from  $S_D = C_D = 1$  to  $S_D = C_D = 0$ .
6. Clock pulse fall time must be  $< 100 \text{ ns}$ .

NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL  
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL

**TYPICAL RESISTANCE VALUES**

R1 = 600 $\Omega$	R5 = 550 $\Omega$
R2 = 2 k	R6 = 900 $\Omega$
R3 = 640 $\Omega$	R7 = 700 $\Omega$
R4 = 300 $\Omega$	R8 = 3 k

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC826P Test Limits							MC726P Test Limits							TEST VOLTAGE					Gnd		
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	APPLIED TO PINS LISTED BELOW:							
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		Min	Max	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>		V <sub>off</sub>	V <sub>CC</sub>
Input Current	2I <sub>in</sub> I <sub>in</sub>	2	-	1200	-	1200	-	1140	μAdc	-	1000	-	1000	-	940	μAdc	2	-	3, 13	-	11	4		
		3	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	3	-	12	-	-	-		
		9	-	-	-	-	-	-	μAdc	-	-	-	-	-	-	μAdc	9	-	-	-	-	-		
		12	-	-	-	-	-	-	μAdc	-	-	-	-	-	-	μAdc	12	-	-	-	-	-		
		13	-	↓	-	↓	-	↓	μAdc	-	↓	-	↓	-	↓	μAdc	-	13	-	9	↓	↓		
Output Current	I <sub>A5</sub>	6	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.5	-	mAdc	-	6, 12	9	-	11	4		
		10	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.5	-	mAdc	-	9, 10	12	-	11	4		
Saturation Voltage	V <sub>CE(sat)</sub>	8	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	12	-	9	11	4		
		6*#	-	↓	-	↓	-	↓	mVdc	-	↓	-	↓	-	↓	mVdc	-	13	-	3	↓	↓		
		6*#	-	-	-	-	-	-	mVdc	-	-	-	-	-	-	mVdc	-	-	-	3, 13	-	-		
		6*##	-	-	-	-	-	-	mVdc	-	-	-	-	-	-	mVdc	-	3, 13	-	-	-	-		
		10	-	-	-	-	-	-	mVdc	-	-	-	-	-	-	mVdc	-	3, 13	-	12	-	-		
		10*##	-	-	-	-	-	-	mVdc	-	-	-	-	-	-	mVdc	-	3	-	13	-	-		
		10*#	-	-	-	-	-	-	mVdc	-	-	-	-	-	-	mVdc	-	3, 13	-	-	↓	↓		
10*##	-	↓	-	↓	-	↓	μAdc	-	↓	-	↓	-	↓	μAdc	-	-	-	3, 13	↓	↓				

Pins not listed are left open.

# Pin 9 HIGH

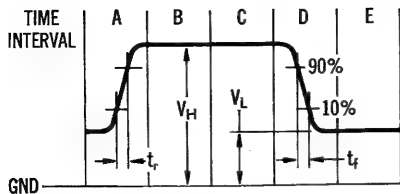
## Pin 12 HIGH

} Set by momentary application of V<sub>BOT</sub> prior to the application of the negative-going clock pulse.

\* Clock Pulse to pin 2, see Figure 1.

@ Test Temperature		TEST VOLTAGE VALUES				
		(Volts)				
		V <sub>I</sub> n	V <sub>o</sub> n	V <sub>B</sub> OT	V <sub>o</sub> ff	V <sub>CC</sub>
MC826P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC726P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

- A. Voltage applied to Clock pin is raised to  $V_H$ .  $t_r$  is not critical but should be  $< 1.0 \mu s$ .
- B. Biases of all other inputs are applied.  $V_{CC}$  is applied without interruption throughout the testing.
- C. Apply momentary ground (when applicable).
- D. Clock pulse is allowed to fall to  $V_L$ .  $t_f$  must remain within 10 ns minimum and 100 ns maximum.
- E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

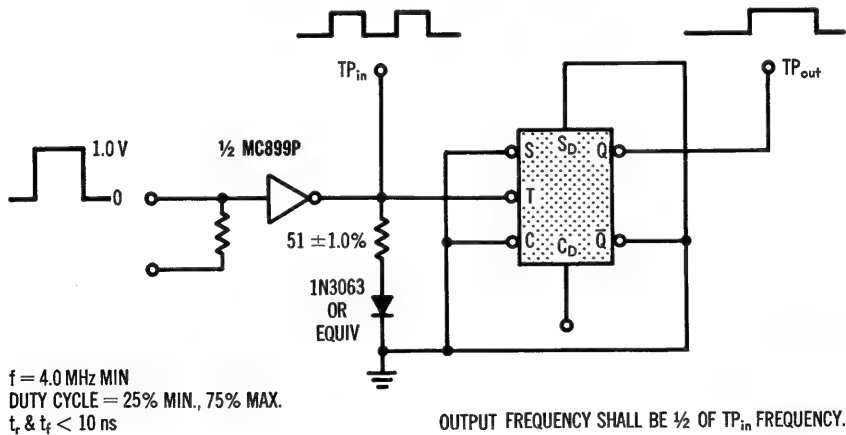
MC826P

$T_A$	$V_L$	$V_H$
+ 25°C	+0.500 V $\pm$ 2.0 mV	+0.930 V $\pm$ 2.0 mV
0°C	+0.570 V $\pm$ 2.0 mV	+0.980 V $\pm$ 2.0 mV
+ 75°C	+0.450 V $\pm$ 2.0 mV	+0.840 V $\pm$ 2.0 mV

MC726P

$T_A$	$V_L$	$V_H$
+ 25°C	+ 0.460 V $\pm$ 2.0 mV	+0.900 V $\pm$ 2.0 mV
+ 15°C	+ 0.475 V $\pm$ 2.0 mV	+0.915 V $\pm$ 2.0 mV
+ 55°C	+ 0.430 V $\pm$ 2.0 mV	+0.850 V $\pm$ 2.0 mV

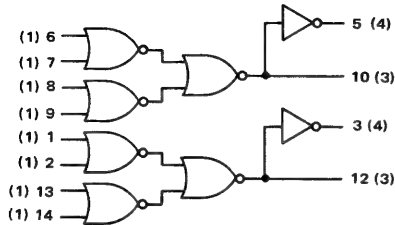
FIGURE 2 — TOGGLE MODE TEST CIRCUIT



DUAL EXCLUSIVE  
"OR-NOR" GATE

PLASTIC mW MRTL MC700P/800P series

MC764P • MC864P



$$12 = (1 + 2) \cdot (13 + 14)$$

$$3 = \bar{1} \cdot \bar{2} + \bar{13} \cdot \bar{14}$$

$t_{pd} = 65$  ns (Pins 5 and 3)  
 $t_{pd} = 35$  ns (Pins 10 and 12)  
 $P_D = 25$  mW

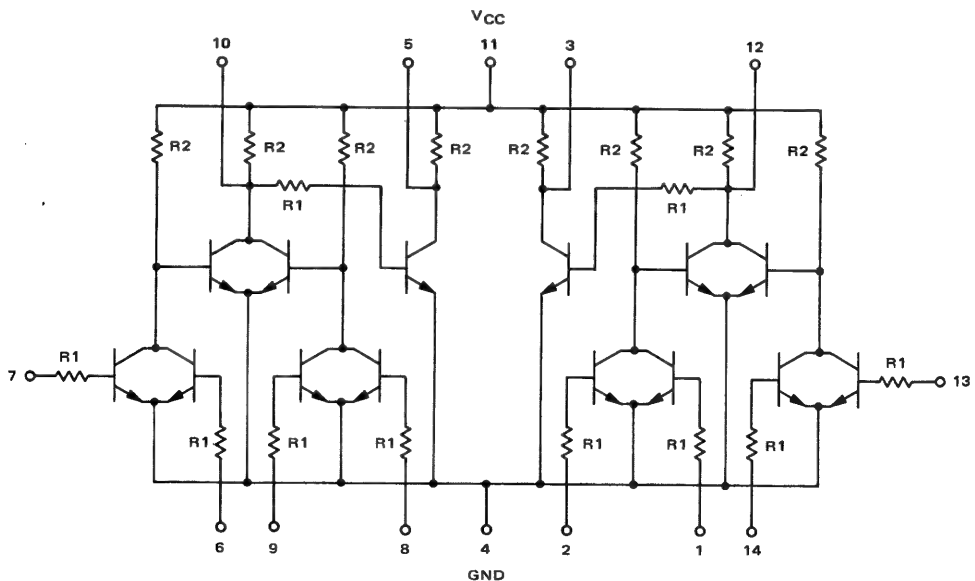
Number in Parenthesis Indicates Loading Factor.

MC764P/864P is a dual multi-purpose device. Types of recommended utilization include:

**Dual Exclusive OR-NOR Gate**, when  $6 = \bar{8}$  and  $7 = \bar{9}$ , then  $10 = 6 \cdot \bar{7} + \bar{6} \cdot 7$  (This equals the sum when used as a Half-Adder) and  $5 = 6 \cdot 7 + \bar{6} \cdot \bar{7}$ .

**Dual Data Distributor**, with data on 6 and 9, control on 7 and control on 8 so that  $10 = 9 \cdot 7 + 6 \cdot \bar{7}$  and  $5 = 9 \cdot 7 + \bar{6} \cdot \bar{7}$ .

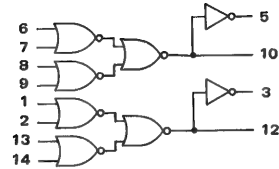
**Dual Gated R-S Flip-Flop**, by connecting the non-inverted output back to an input. When pin 10 is connected to pin 9 then  $\bar{10} = 5 = \bar{6} \cdot \bar{7}$  and  $\bar{5} = 10 = 8 \cdot (6 + 7)$ . Pin 10 will remain in its previous state ( $10^{n+1} = 10^n$ ) whenever the input configuration is  $8 \cdot (6 + 7)$ . Another name for the flip-flop, then, is a  $\bar{R}\bar{1}R2$ -S flip-flop.



TYPICAL RESISTANCE VALUES

$R1 = 1.5$  k $\Omega$   
 $R2 = 3.6$  k $\Omega$

Test procedures are shown for only one gate. The other gate is tested in the same manner.



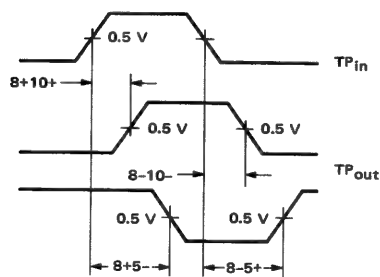
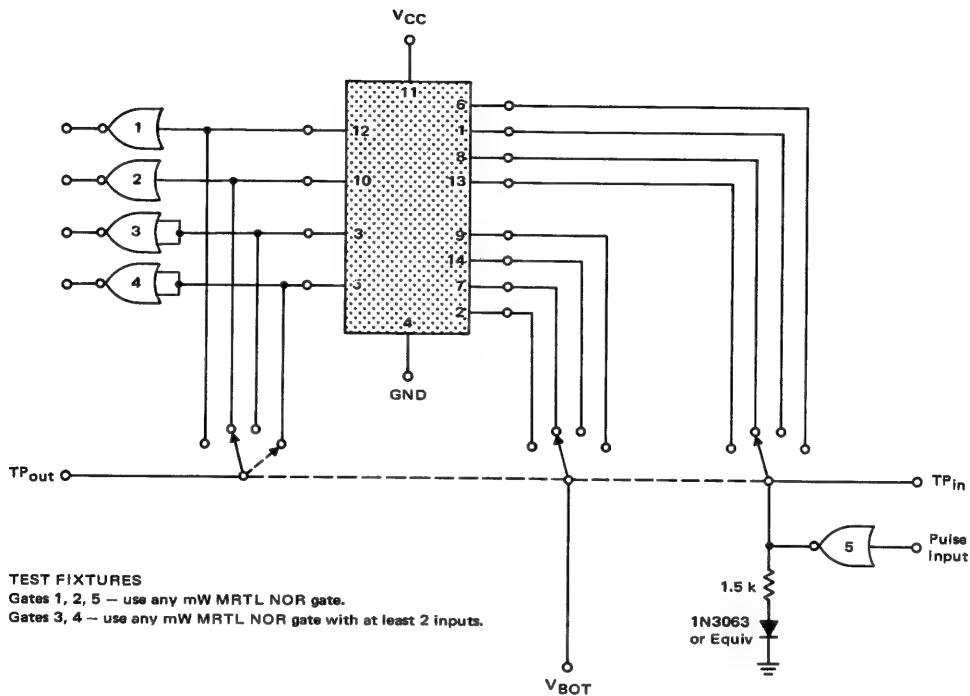
@ Test Temperature				TEST VOLTAGE VALUES					
				(Volts)					
				V <sub>In</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	
MC864P	{	0°C	0.880	0.850	1.80	0.500	3.60		
		+25°C	0.830	0.800	1.80	0.460	3.60		
		+75°C	0.740	0.710	1.80	0.400	3.60		
MC764P	{	+15°C	0.865	0.865	1.80	0.475	3.60		
		+25°C	0.850	0.850	1.80	0.460	3.60		
		+55°C	0.800	0.800	1.80	0.430	3.60		
TEST LIMITS				TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					
C	+55°C		Unit	V <sub>In</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	Gnd
Max	Min	Max							
150	-	150	μAdc	6	-	7	-	11	4
↓	-	↓	↓	7	-	6	-	↓	↓
-	-	-	-	8	-	9	-	-	-
-	-	-	-	9	-	8	-	-	-
-	640	-	μAdc	-	5	-	6,7,8,9	11	4
-	480	-	↓	-	7,8,10	-	-	↓	↓
-	480	-	↓	-	6,9,10	-	-	↓	↓
300	-	320	mVdc	-	6,7,8,9	-	-	11	4
↓	-	↓	↓	-	8,9	-	6,7	↓	↓
-	-	-	-	-	6,7	-	8,9	↓	↓
-	-	-	-	-	-	-	6,7,8,9	↓	↓
80	-	-	ns	Pulse In	Pulse Out	9	-	11	4
60	-	-	↓	8	5	9	-	↓	↓
65	-	-	↓	↓	5	9	-	↓	↓
35	-	-	↓	↓	10	7	-	↓	↓
	-	-	↓	↓	10	7	-	↓	↓

Ground unused input pins. Other pins not listed are left open.

MC764P, MC864P (continued)



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



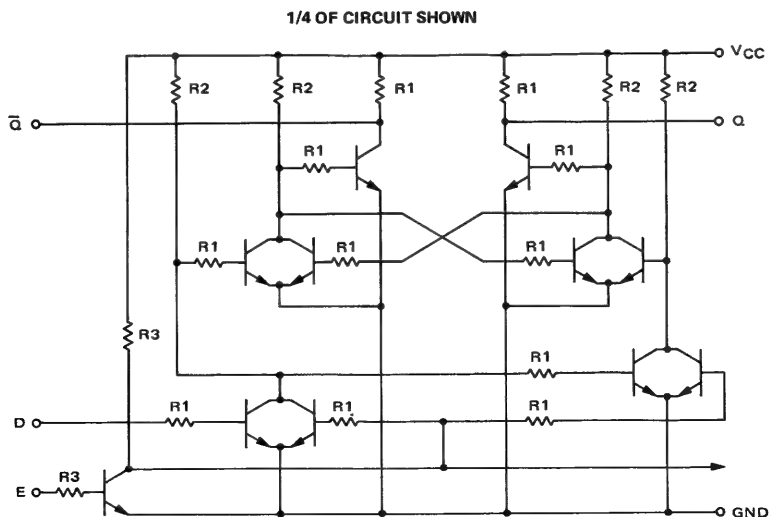
INPUT PULSE  
 $f = 4.0 \text{ MHz}$   
 $PW = 100 \text{ ns}$   
 $PH = 1.5 \text{ V}$   
 $t_r = t_f \leq 10 \text{ ns}$

## PLASTIC mW MRTL MC700P/800P series

The diagram illustrates a 4-bit parallel adder circuit. It features four identical stages, each processing a 4-bit input (D1, D2, D3, D4) and a 4-bit input (E). The circuit uses 9013 CMOS inverters and 9011 CMOS NAND gates. The outputs are 8-bit numbers: 2 Q1 (9), 1 Q1 (9), 7 Q2 (9), 8 Q2 (9), 10 Q3 (9), 11 Q3 (9), 15 Q4 (9), and 14 Q4 (9).

The MC767P/867P Quad Latch is designed for use in any application requiring temporary storage. A common enable line allows only the desired information to be "clocked in." When the level of the enable line is high, the output of each latch will be synonymous with the data input to that latch. When the enable line level goes low, the output will remain at the previous level, independent of any changes at the input. The MC767P/867P is available in a 16-pin dual in line plastic package.

E	D	$Q_{n+1}$	$\bar{Q}_{n+1}$
0	0	$Q_n$	$\bar{Q}_n$
0	1	$Q_n$	$\bar{Q}_n$
1	0	0	1
1	1	1	0

$$\bullet \text{ Avg } t_{pd} = \frac{t_{on} + t_{off}}{2}$$


**TYPICAL RESISTANCE VALUES**  
**R1 = 1.5 k      R3 = 750  $\Omega$**   
**R2 = 3.6 k**

## ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one latch. The other latches are tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC867P Test Limits							MC767P Test Limits							TEST VOLTAGE VALUES (Volts)					Gnd
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	
			Test																			
Input Current	I <sub>in</sub>	3	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	3	-	-	-	13	4,5
	2 I <sub>in</sub>	5	-	300	-	280	-	280	μAdc	-	300	-	300	-	300	μAdc	5	-	-	-	13	4
Output Current	I <sub>A0</sub>	1	-1.28	-	-1.28	-	-1.20	-	mAdc	-1.28	-	-1.28	-	-1.28	-	mAdc	3,5	1	-	-	13	4
		2	-1.28	-	-1.28	-	-1.20	-	mAdc	-1.28	-	-1.28	-	-1.28	-	mAdc	5	2	-	-	13	3,4
Saturation Voltage	V <sub>CE(sat)</sub>	1	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	5	-	-	-	13	3,4
		2	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		3,5	-	-	-	↓	4
		1	-	-	-	-	-	-		-	-	-	-	-	-		3,5*	-	-	-	↓	3,4,5*
		2	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		3,5**	-	-	-	↓	3,4,5**
Power Supply Drain Current	I <sub>PD</sub>	13	-	-	-	35	-	-	mAdc	-	-	-	35	-	-	mAdc	-	-	-	-	13	4,5
Switching Times																	Pulse In	Pulse Out				
	t <sub>3+1+</sub>	1	-	-	-	75	-	-	ns	-	-	-	75	-	-	ns	3	1	5	-	13	4
	t <sub>3-1-</sub>	1	-	-	-	70	-	-	↓	-	-	-	70	-	-	↓	1	1	↓	-	↓	↓
	t <sub>3+2-</sub>	2	-	-	-	90	-	-	↓	-	-	-	90	-	-	↓	2	2	↓	-	↓	↓
	t <sub>3-2+</sub>	2	-	-	-	60	-	-	↓	-	-	-	60	-	-	↓	2	2	↓	-	↓	↓

Ground inputs of latches not under test. Other pins not listed are left open.

\*A negative pulse from V<sub>in</sub> to ground is applied to pin 5, then 2.0 ms later a positive pulse from ground to V<sub>in</sub> is applied to pin 3 for measurement of V<sub>CE</sub> on pin 1.

\*\*A negative pulse from V<sub>in</sub> to ground is applied to pin 5, then 2.0 ms later a positive pulse from V<sub>in</sub> to ground is applied to pin 3 for measurement of V<sub>CE</sub> on pin 2.

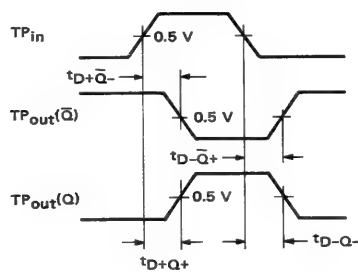
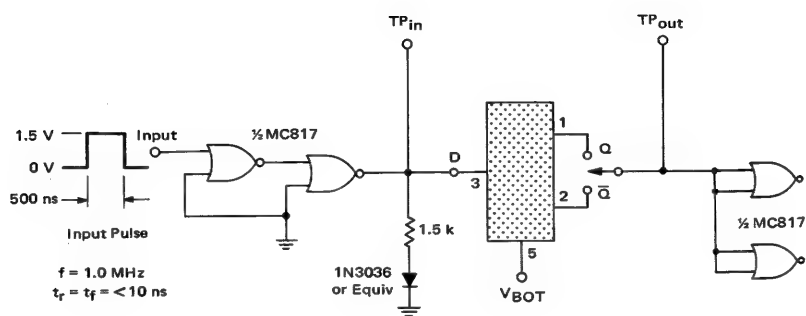
@ Test Temperature

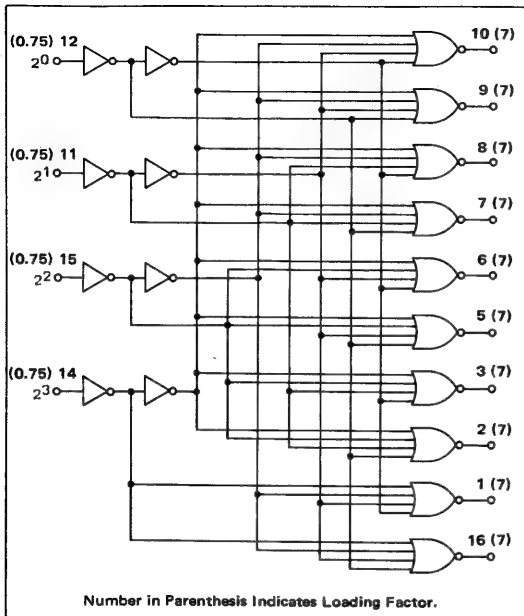
MC867P { 0°C  
+25°C  
+75°C

MC767P { +15°C  
+25°C  
+55°C

TEST VOLTAGE VALUES (Volts)				
V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>
0.880	0.850	1.80	0.500	3.60
0.830	0.800	1.80	0.460	3.60
0.740	0.710	1.80	0.400	3.60
0.865	0.865	1.80	0.475	3.60
0.850	0.850	1.80	0.460	3.60
0.800	0.800	1.80	0.430	3.60

### SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



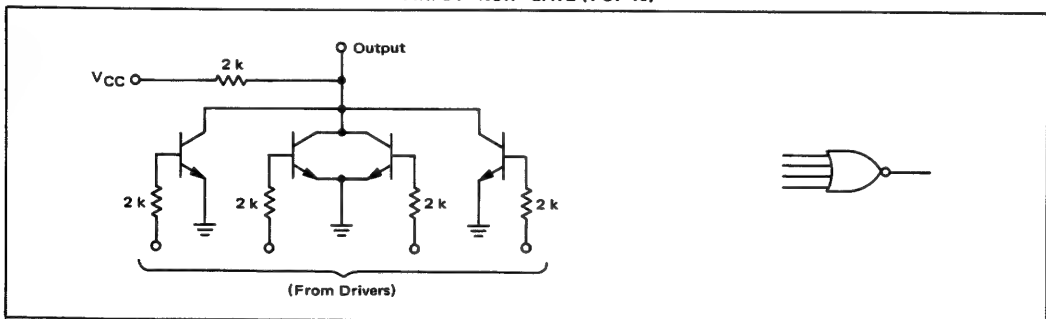
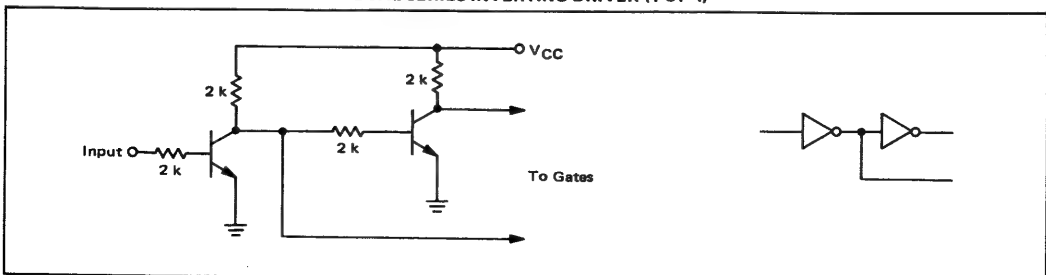
**MC770P • MC870P\***

The MC770P/870P is a monolithic BCD to decimal decoder consisting of eight inverters and ten 4-input NOR gates which are utilized to convert binary coded decimal (8-4-2-1) input to an output, via the appropriate one of ten output lines.

		TRUTH TABLE													
		INPUT (BCD)				OUTPUT (DECIMAL)									
Value	Pin No.	2 <sup>3</sup>	2 <sup>2</sup>	2 <sup>1</sup>	2 <sup>0</sup>	0	1	2	3	4	5	6	7	8	9
Logic Level		14	15	11	12	10	9	8	7	6	5	3	2	1	16
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0
0	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0
0	1	0	1	1	0	0	0	0	0	0	0	0	0	1	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1
0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

$t_{pd} = 36 \text{ ns}$

$P_D = 100 \text{ mW typ (All inputs high)}$

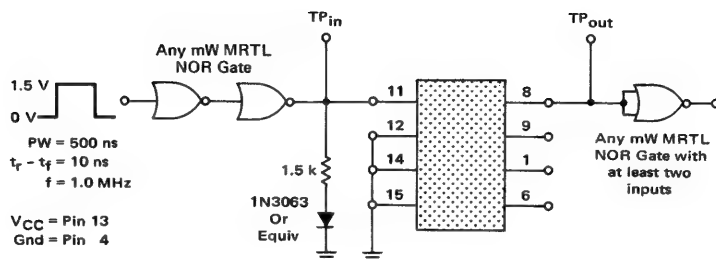
**4-INPUT "NOR" GATE (1-OF-10)****DUAL SERIES INVERTING DRIVER (1-OF-4)**

\*P suffix = 16 pin dual-in-line plastic package, Case 612.

## MC770P, MC870P (continued)

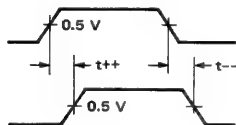
\*\*Test shown is for one output only. All nine outputs, excepting the one which is "ON" according to the truth table, are to be tested for all usable input configurations shown in the truth table — a total of 90 tests.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



Switching Circuit indicates one input and one output. Other input and output combinations are tested in a similar manner.

Load and driving gates must be of same series as unit under test.

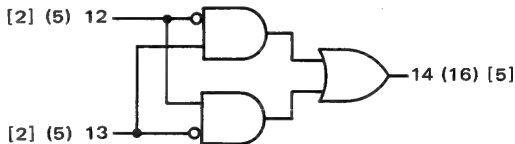
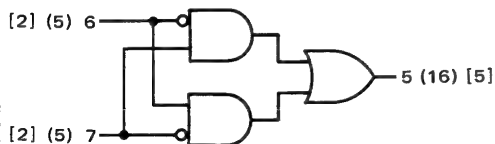
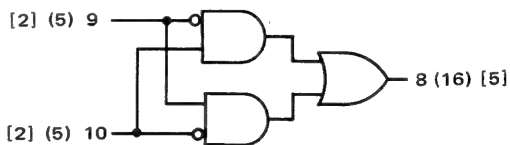
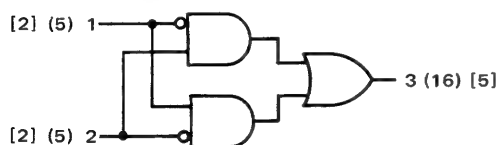


# QUAD EXCLUSIVE OR GATES

# PLASTIC MRTL MC700P/800P series

## MC771P • MC871P

Four gate arrays designed to provide the Exclusive OR function. The output is high only if one input is high and all other inputs are low.



### POSITIVE LOGIC

$$3 = 1 \cdot \bar{2} + \bar{1} \cdot 2$$

$$t_{pd} = 12 \text{ ns typ}$$

$$P_D = 87 \text{ mW typ}$$

NUMBER IN PARENTHESIS INDICATES  
LOADING FACTOR FOR mW MRTL

NUMBER IN BRACKETS INDICATES  
LOADING FACTOR FOR MRTL

## ELECTRICAL CHARACTERISTICS

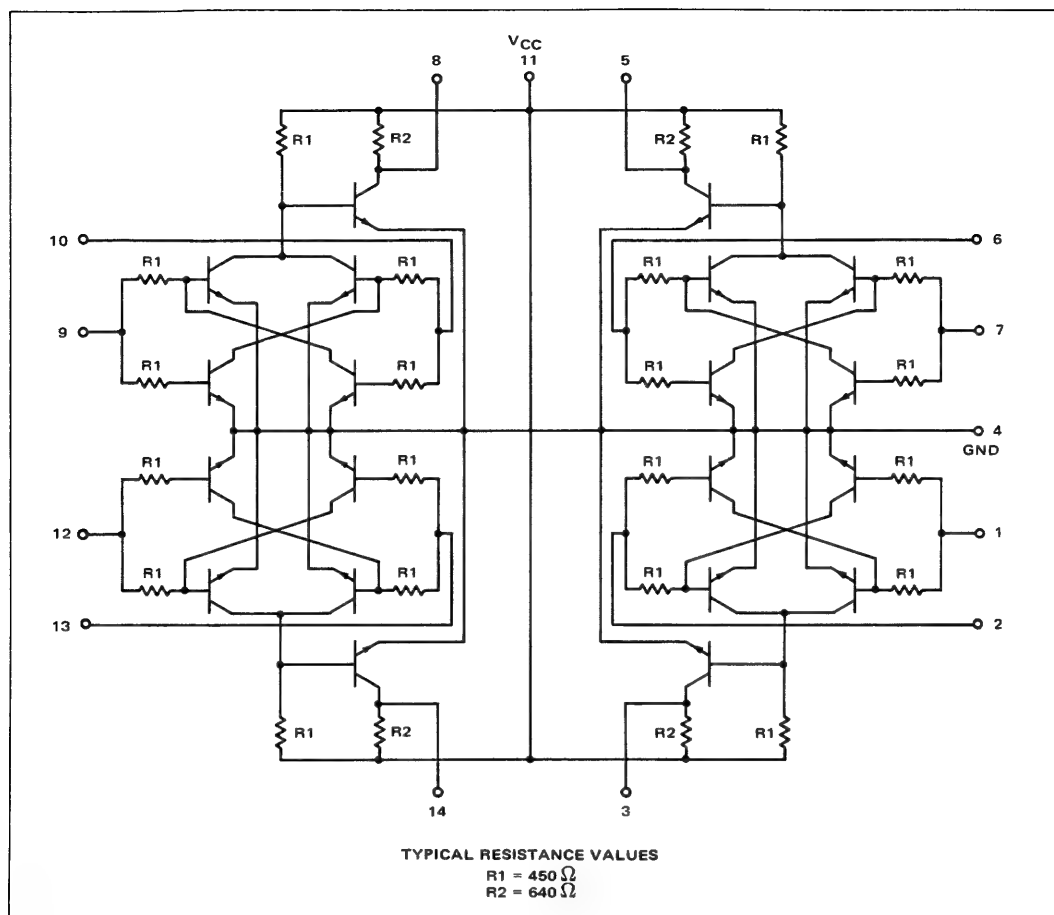
Test procedures are shown for one gate only.  
The other gates are tested in the same manner.

		TEST VOLTAGE VALUES				
		(Volts)				
@ Test Temperature		V <sub>in</sub>	V <sub>on</sub>	V <sub>off</sub>	V <sub>st</sub>	V <sub>cc</sub>
MC871P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
	+15°C	0.865	0.865	1.80	0.475	3.60
MC771P	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

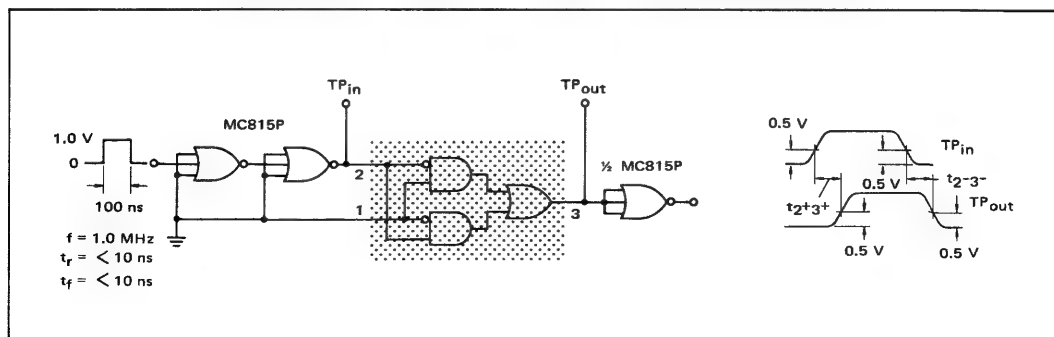
Characteristic	Symbol	Pin Under Test	MC871P Test Limits								MC771P Test Limits								TEST VOLTAGE						Gnd
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	APPLIED TO PINS LISTED BELOW:								
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		Min	Max	V <sub>in</sub>	V <sub>on</sub>	V <sub>off</sub>	V <sub>st</sub>	V <sub>cc</sub>		
Input Current	2I <sub>in</sub>	1	-	1.2	-	1.2	-	1.1	mAdc	-	1.00	-	1.00	-	0.94	mAdc	1	-	2	-	11	4			
		2	-	1.2	-	1.2	-	1.1	mAdc	-	1.00	-	1.00	-	0.94	mAdc	2	-	1	-	11	4			
Output Current	I <sub>A5</sub>	3	3.00	-	3.00	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	1,3	-	2	11	4			
		3	3.00	-	3.00	-	3.00	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	2,3	-	1	11	4			
Output Voltage	V <sub>out</sub>	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	-	-	1,2	11	4			
		3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	-	1,2	-	11	4			
Switching Time	t	1-3- 1-3+ 2-3+ 2-3-	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	Pulse In	Pulse Out	-	-	11	4			
			-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	1	2	3	-	-	4			
			-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	2	2	3	-	-	4			
			-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	2	2	3	-	-	4			

Ground inputs of gates not under test. Other pins not listed are left open.





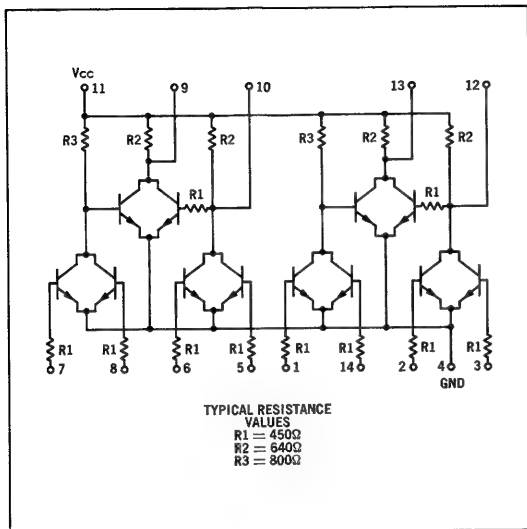
### SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



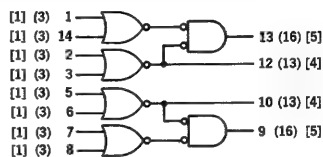
# DUAL HALF-ADDERS

PLASTIC MRTL MC700P/800P series

## MC775P • MC875P



Two half-adder devices in a single package. Each device can be used to supply the SUM and CARRY operations on two input signals. E.g., if the inputs are applied to pins 1 and 14, and their complements to pins 2 and 3, the SUM of the inputs appears on pin 13 while the CARRY appears on pin 12.

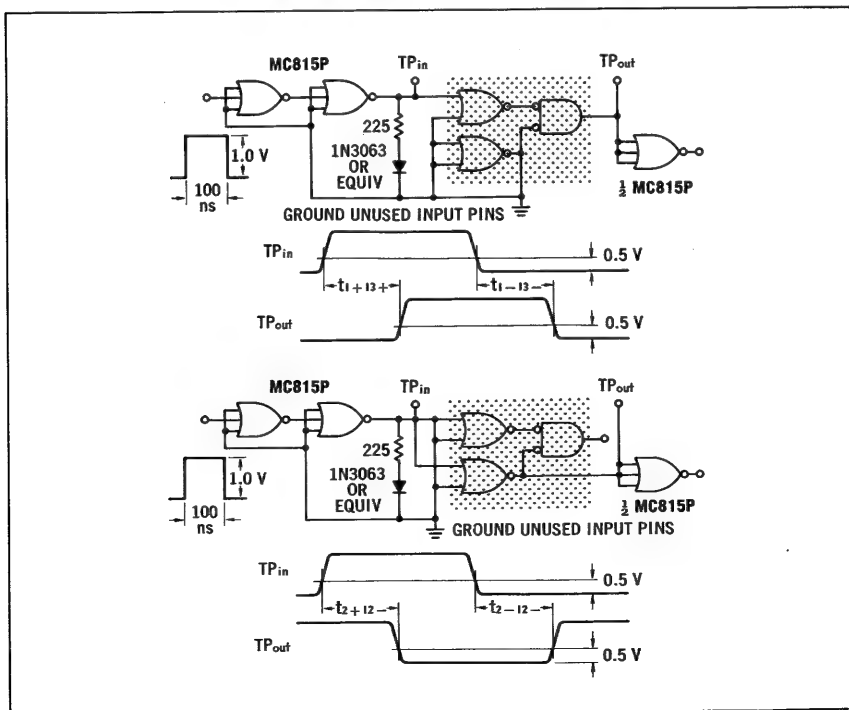


IF:  $2 = \overline{1}$ , &  $3 = \overline{14}$   
 THEN:  $12 = 1 \cdot 14$ , &  $13 = 1 \cdot \overline{14} + \overline{1} \cdot 14$

$t_{pd} = 20 \text{ ns typ}$   
 $P_D = 120 \text{ mW typ}$

NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL  
 NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL

### SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



## ELECTRICAL CHARACTERISTICS

Test procedures are shown for one half-adder only.  
The other half-adder is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC875P Test Limits							MC775P Test Limits							TEST VOLTAGE					Gnd
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	APPLIED TO PINS LISTED BELOW:					
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	
Input Current	I <sub>in</sub>	1	-	600	-	600	-	570	μA <sub>dc</sub>	-	500	-	500	-	470	μA <sub>dc</sub>	1	-	14	-	11	4
		2	-		-		-			-		-		-		-	2	-	3	-		
		3	-		-		-			-		-		-		-	3	-	2	-		
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	14	-	14	-	↓	↓
Output Current	I <sub>A4</sub>	12	2.4	-	2.4	-	2.28	-	mA <sub>dc</sub>	-	-	-	-	-	-	-	-	12	-	2, 3	11	4
	I <sub>A5</sub>	13	3.0	-	3.0	-	2.85	-	↓	2.65	-	2.65	-	2.5	-	mA <sub>dc</sub>	-	1, 2, 13	-	-		↓
	I <sub>A5</sub>	13	3.0	-	3.0	-	2.85	-	↓	2.65	-	2.65	-	2.5	-	mA <sub>dc</sub>	-	3, 13, 14	-	-	↓	
Output Voltage	V <sub>out</sub>	12	-	500	-	400	-	400	mV <sub>dc</sub>	-	400	-	300	-	320	mV <sub>dc</sub>	-	2	-	-	11	4
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-		
		13	-		-		-		↓	-		-		-		↓	-	12	1, 13	-	↓	↓
Saturation Voltage	V <sub>CE(sat)</sub>	12	-	400	-	300	-	350	mV <sub>dc</sub>	-	300	-	290	-	320	mV <sub>dc</sub>	-	-	2	-	11	4
		12	-		-		-			-		-		-			-	-	3	-		
		13	-		-		-		↓	-		-		-			-	-	1, 14	2, 3		↓
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	2, 3	1, 14	↓	↓
Switching Time	t	2+12-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	Pulse In	Pulse Out	-	-	11	4
		2-12+	-	-	-	30	-	-	↓	-	-	-	30	-	-	↓	2	12	-	-		4
		1+13+	-	-	-	36	-	-		-	-	-	36	-	-		2	12	-	-		4
		1-13-	-	-	-	36	-	-		-	-	-	36	-	-		1	13	-	-	↓	4, 12
									↓	-	-	-	36	-	-	↓	1	13	-	-	↓	4, 12

Ground inputs of half-adder not under test. Other pins not listed are left open.

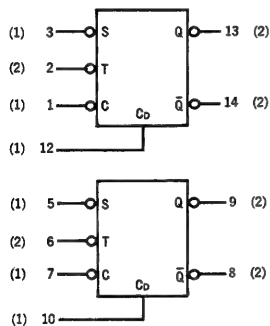
	@ Test Temperature	TEST VOLTAGE VALUES (Volts)				
		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>
MC875P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC775P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

DUAL J-K FLIP-FLOPS

PLASTIC mW MRTL MC700P/800P series

# MC776P • MC876P

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



$f_{\text{max}} = 3 \text{ MHz min}$   
 $P_D = 41 \text{ mW (Only Clock Input High)}$   
 $29 \text{ mW (All Inputs Low)}$

NUMBER IN PARENTHESES  
 INDICATES LOADING FACTOR

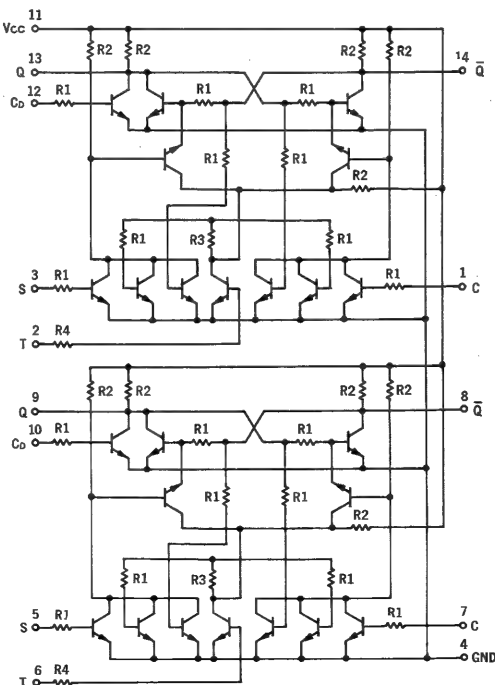
## CLOCKED INPUT OPERATION①

$t_n$ ②		$t_{n+1}$ ③	
S	C	Q	$\bar{Q}$
1	1	$Q_n$ ④	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$Q_n$	$\bar{Q}_n$ ④

① Direct input ( $C_o$ ) must be low.

② The time period prior to the negative transition of the clock pulse is denoted  $t_n$  and the time period subsequent to this transition is denoted  $t_{n+1}$ .

③  $Q_n$  is the state of the Q output in the time period  $t_n$ .



TYPICAL RESISTANCE  
 VALUES  
 $R1 = 1.5k$   $R3 = 3.0k$   
 $R2 = 3.6k$   $R4 = 750\Omega$

# ELECTRICAL CHARACTERISTICS

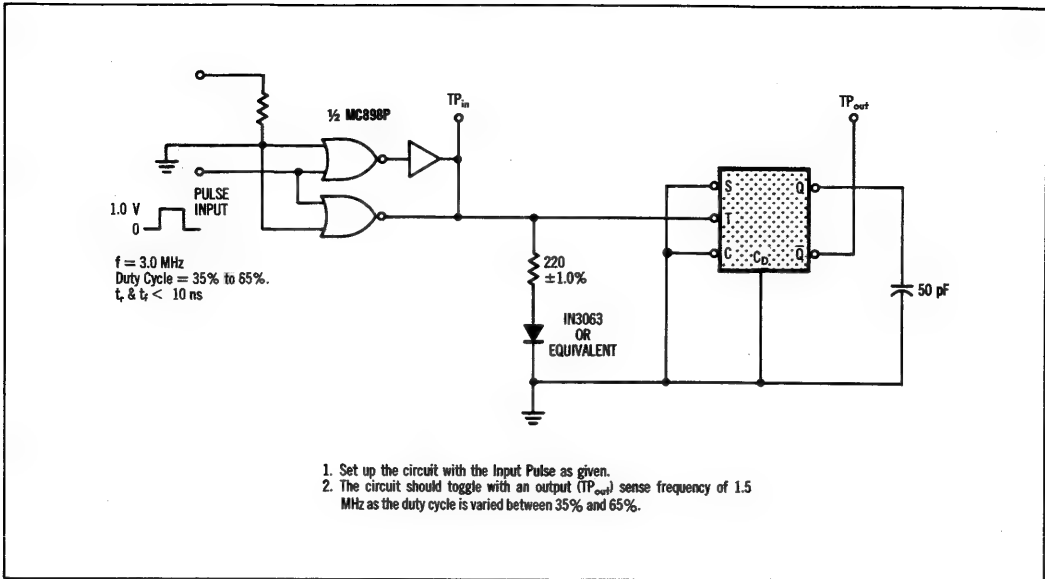
Test procedures are shown for one flip-flop only.  
The other flip-flop is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC876P Test Limits							MC776P Test Limits							TEST VALUES						
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	APPLIED TO PINS LISTED BELOW:						
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	I <sub>O</sub>	Gnd
Input Current	I <sub>in</sub>	1	-	150	-	140	-	140	μA <sub>dc</sub>	-	150	-	150	-	150	μA <sub>dc</sub>	1	-	13	-	11	-	4
	2 I <sub>in</sub>	2	-	300	-	280	-	280	μA <sub>dc</sub>	-	300	-	300	-	300	μA <sub>dc</sub>	2	-	1, 3	-	↓	-	↓
	I <sub>in</sub>	3	-	150	-	140	-	140	μA <sub>dc</sub>	-	150	-	150	-	150	μA <sub>dc</sub>	3	-	14	-	↓	-	↓
	I <sub>in</sub>	12	-	150	-	140	-	140	μA <sub>dc</sub>	-	150	-	150	-	150	μA <sub>dc</sub>	12	-	14	-	↓	-	↓
Output Current	I <sub>A2</sub>	13	320	-	320	-	300	-	μA <sub>dc</sub>	320	-	320	-	320	-	μA <sub>dc</sub>	-	13	1	12	11	-	4, 14 §
		14	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	-	3, 12	-	↓	-	↓	
		14	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	-	12, 14	3	-	↓	-	↓
Output Voltage	V <sub>out</sub>	13	-	400	-	350	-	300	mV <sub>dc</sub>	-	400	-	300	-	320	mV <sub>dc</sub>	-	12	-	-	↓	-	4, 14
		13	-	↓	-	↓	-	↓	mV <sub>dc</sub>	-	↓	-	↓	-	↓	mV <sub>dc</sub>	-	14	-	-	↓	-	4, 13 §
		13*†	-	-	-	-	-	-	mV <sub>dc</sub>	-	-	-	-	-	-	mV <sub>dc</sub>	-	1, 3	-	-	↓	-	4, 12
		13*#	-	-	-	-	-	-	mV <sub>dc</sub>	-	-	-	-	-	-	mV <sub>dc</sub>	-	1	-	3	↓	-	↓
		13*#	-	-	-	-	-	-	mV <sub>dc</sub>	-	-	-	-	-	-	mV <sub>dc</sub>	-	-	-	1, 3	↓	-	↓
Saturation Voltage	V <sub>CE(sat)</sub>	13	-	250	-	250	-	250	mV <sub>dc</sub>	-	220	-	230	-	320	mV <sub>dc</sub>	-	-	12	-	11	-	4, 14
		13	-	↓	-	↓	-	↓	mV <sub>dc</sub>	-	↓	-	↓	-	↓	mV <sub>dc</sub>	-	-	-	-	↓	-	4, 13 §
		14	-	↓	-	↓	-	↓	mV <sub>dc</sub>	-	↓	-	↓	-	↓	mV <sub>dc</sub>	-	-	-	12	↓	-	4, 14 §
Turn On Voltage	V <sub>on</sub>	13*#	850	-	800	-	710	-	mV <sub>dc</sub>	865	-	850	-	800	-	mV <sub>dc</sub>	-	1, 3	-	-	11	13	4, 12
		13*†	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	mV <sub>dc</sub>	-	3	-	1	↓	↓	↓
		13*†	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	mV <sub>dc</sub>	-	-	-	1, 3	↓	↓	↓

\* Clock Pulse to pin 2  
† Pin 13 = LOW } Set by a momentary ground prior to the  
# Pin 14 = LOW } application of the negative-going clock.  
§ ground thru diode (cathode to ground).  
Ground inputs of flip-flop not under test.  
Other pins not listed are left open.

@ Test Temperature		TEST VALUES					
		(Volts)					$\mu A$
		$V_{in}$	$V_{on}$	$V_{BOT}$	$V_{off}$	$V_{CC}$	
{	0°C	0.880	0.850	1.80	0.500	3.60	270
	+25°C	0.830	0.800	1.80	0.460	3.60	290
	+75°C	0.740	0.710	1.80	0.400	3.60	255
	+15°C	0.865	0.865	1.80	0.475	3.60	270
	+25°C	0.850	0.850	1.80	0.460	3.60	270
{	+ 55°C	0.800	0.800	1.80	0.430	3.60	270

TOGGLE MODE TEST CIRCUIT



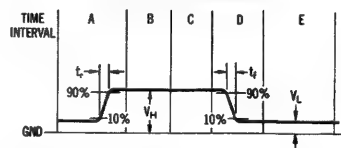
CLOCK PULSE

MC776P		
$T_A$	$V_L$	$V_H$
15°C	0.475 V	0.915 V
25°C	0.460 V	0.900 V
55°C	0.430 V	0.850 V

MC876P		
$T_A$	$V_L$	$V_H$
0°C	0.50 V	0.900 V
25°C	0.46 V	0.850 V
75°C	0.40 V	0.760 V

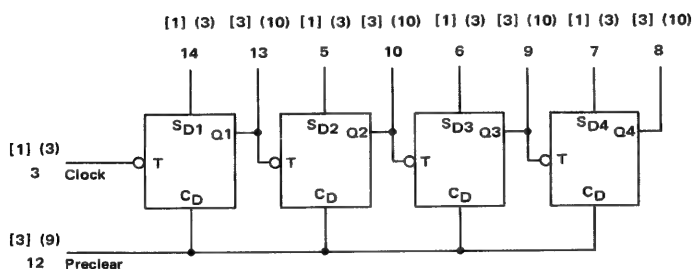
All values are  $\pm 2.0\text{mV}$

CLOCK PULSE DEFINITION



**MC777P • MC877P**

This monolithic binary counter has outputs corresponding to a standard 8-4-2-1 binary code, with individual presets and a common preclear input.



## DECODING LOGIC

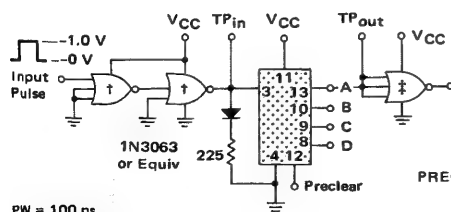
0	$\bar{A} \bar{B} \bar{C} \bar{D}$
1	$A \bar{B} \bar{C} \bar{D}$
2	$\bar{A} B \bar{C} \bar{D}$
3	$A B \bar{C} \bar{D}$
4	$\bar{A} \bar{B} C \bar{D}$
5	$A \bar{B} C \bar{D}$
6	$\bar{A} B C \bar{D}$
7	$A B C \bar{D}$
8	$\bar{A} \bar{B} C D$
9	$A \bar{B} C D$
10	$\bar{A} B C D$
11	$A B C D$
12	$\bar{A} \bar{B} C \bar{D}$
13	$A \bar{B} C \bar{D}$
14	$\bar{A} B C \bar{D}$
15	$A B C \bar{D}$

Numbers in Brackets Indicate MRTL Loading Factor.

Numbers in Parenthesis Indicate mW MRTL Loading Factor.

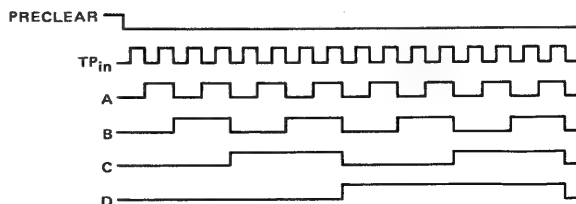
$f_{Tog} = 4.0 \text{ MHz}$   
 $P_D = 180 \text{ mW typ}$

## TOGGLE TEST CIRCUIT AND WAVEFORMS



PW = 100 ns  
 $f = 1.0 \text{ MHz typ}$

† = Any MRTL NOR gate.  
 ‡ = Any MRTL 3-input NOR gate.



## ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only. The other flip-flops are tested in the same manner.

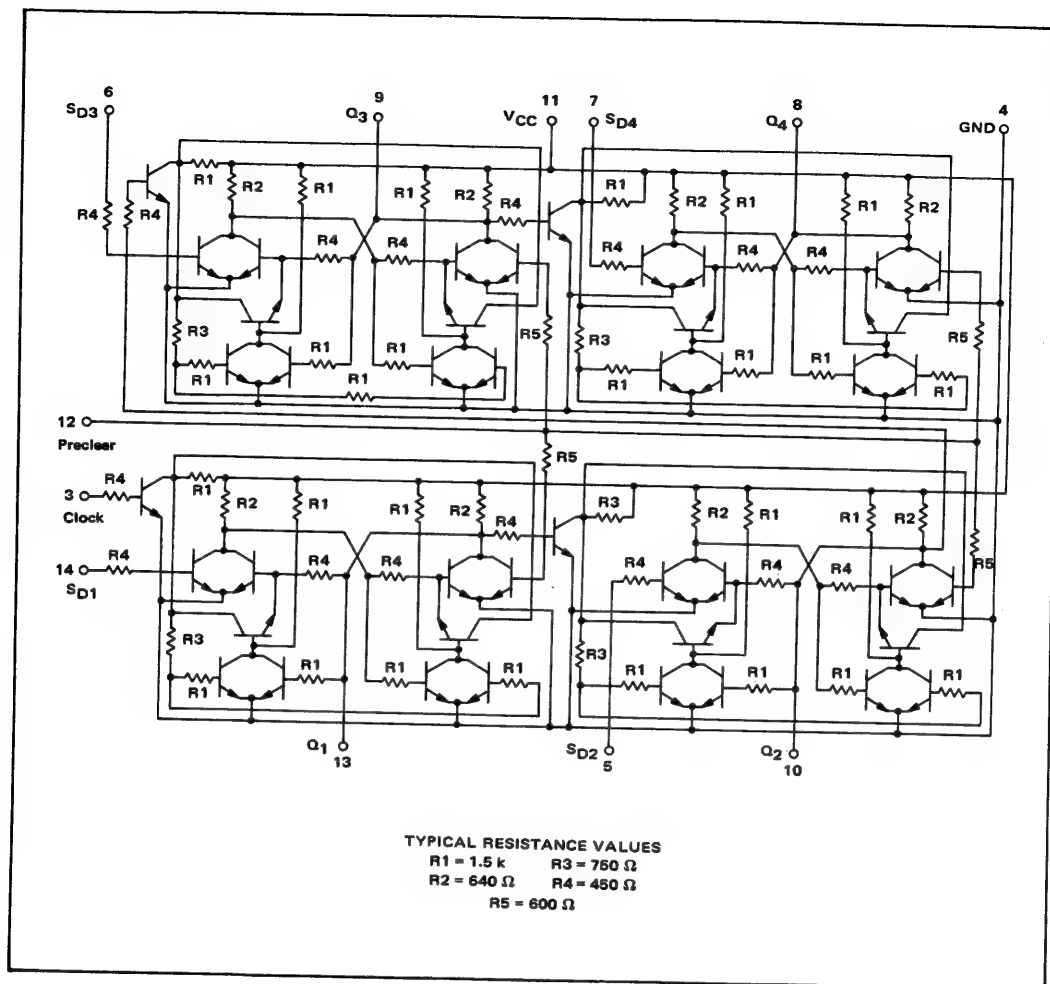
		@ Test Temperature	TEST VOLTAGE VALUES (Volts)					Gnd
			V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	
MC877P	0°C		0.960	0.930	1.80	0.570	3.60	
	+25°C		0.910	0.880	1.80	0.500	3.60	
	+75°C		0.820	0.790	1.80	0.450	3.60	
MC777P	+15°C		0.865	0.865	1.80	0.475	3.60	
	+25°C		0.850	0.850	1.80	0.460	3.60	
	+55°C		0.800	0.800	1.80	0.430	3.60	

Characteristic	Symbol	Pin Under Test	MC877P Test Limits							MC777P Test Limits							TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					Gnd
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max							
Input Current	I <sub>in</sub>	3	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	3	-	-	-	11	4
	I <sub>in</sub>	5	-	600	-	600	-	570	↓	-	500	-	500	-	470	↓	5	-	-	-	↓	↓
	3 I <sub>in</sub>	12	-	1800	-	1800	-	1710	↓	-	1500	-	1500	-	1410	↓	12	-	-	-	↓	↓
Output Current	I <sub>A3</sub>	10	-1.80	-	-1.80	-	-1.71	-	mAdc	-1.65	-	-1.65	-	-1.56	-	mAdc	10	-	5	-	11	4
Output Voltage	V <sub>out</sub>	10	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	-	-	-	11	4.10*
Saturation Voltage	V <sub>CE(sat)</sub>	10	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	-	-	11	4
Power Supply Current Drain	I <sub>PD</sub>	11	-	-	-	80	-	-	mAdc	-	-	-	80	-	-	mAdc	-	-	12	-	11	4
Switching Times	t <sub>3-8+</sub> t <sub>3-8-</sub>	8	-	-	-	100	-	-	ns	-	-	-	100	-	-	ns	Pulse In	Pulse Out	-	-	11	4
																	3	8				
																	3	8				

\*Apply a momentary ground to pin 10 prior to measurement.  
Ground input pins of flip-flops not under test. Other pins not listed are left open.



# MC777P, MC877P (continued)

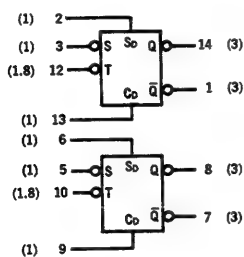


# DUAL TYPE D FLIP-FLOPS

PLASTIC mW MRTL MC700P/800P series

## MC778P • MC878P

The type "D" Flip-Flop is a storage element that stores the state of the S input during negative transitions of the T input. The flip-flop state is not affected by changes in the S input during either the low or the high state of the T input. S<sub>0</sub> and C<sub>0</sub> inputs may be used for asynchronous operation.



### DIRECT INPUT OPERATION<sup>①</sup>

S <sub>0</sub>	C <sub>0</sub>	Q	$\bar{Q}$
0	0	③	③
1	0	1	0
0	1	0	1
1	1	0	0

### CLOCKED INPUT OPERATION<sup>②</sup>

$t_{n-1}$	$t_n$	Q	$\bar{Q}$
S	Q	Q	$\bar{Q}$
1	1	0	1
0	0	1	1

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR

P<sub>0</sub> = 48 mW (Direct Set, S<sub>0</sub>, and Direct Clear, C<sub>0</sub>, Low; all other inputs high)  
35 mW (All inputs Low)

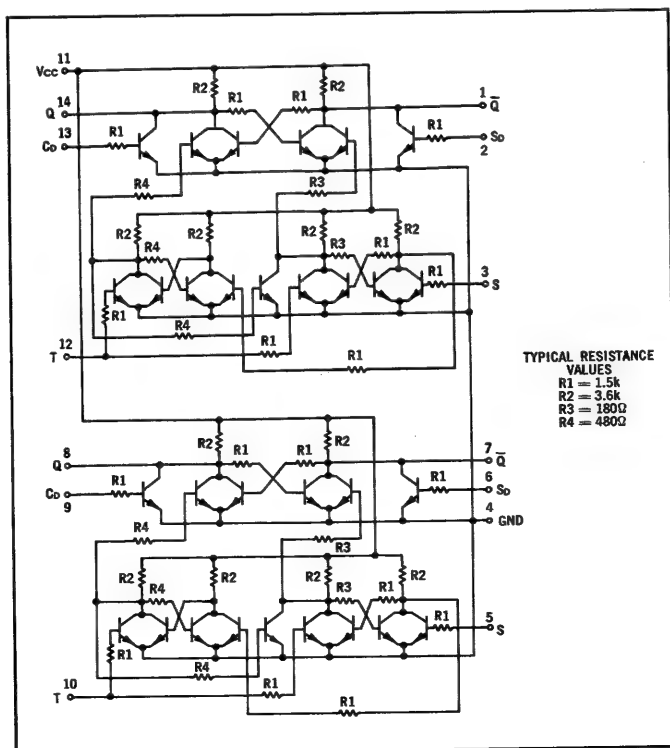
f<sub>rog</sub> = 1 MHz

① Clock (T input) must be high.

② The output state will not change when the input state goes from S<sub>0</sub> = C<sub>0</sub> to S<sub>0</sub> = C<sub>0</sub> = 0. The output state cannot be predetermined in the case where input goes from S<sub>0</sub> = C<sub>0</sub> = 1 to S<sub>0</sub> = C<sub>0</sub> = 0.

③ Direct inputs (S<sub>0</sub> and C<sub>0</sub>) must be low.

④ The time period prior to the negative transition of the clock pulse is denoted t<sub>n</sub>, and the time period subsequent to this transition is denoted t<sub>n+1</sub>.



TYPICAL RESISTANCE VALUES  
R1 = 1.5k  
R2 = 3.6k  
R3 = 180Ω  
R4 = 480Ω

## ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.  
The other flip-flop is tested in the same manner.

@ Test Temperature			TEST VOLTAGE VALUES								
			(Volts)						KΩ ± 1%		
			V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	V <sub>LL</sub>			V <sub>R</sub> *
MC878P	0°C		0.880	0.850	1.80	0.500	3.60	0.45	4.3		
	+25°C		0.830	0.800	1.80	0.460	3.60	0.40	4.3		
	+75°C		0.740	0.710	1.80	0.400	3.60	0.35	4.7		
MC778P	+15°C		0.865	0.865	1.80	0.475	3.80	-	4.6		
	+25°C		0.850	0.850	1.80	0.460	3.60	-	4.8		
	+55°C		0.800	0.800	1.80	0.430	3.60	-	5.0		
Test Limits			TEST VOLTAGE								
+55°C			APPLIED TO PINS LISTED BELOW:								
Min	Max	Unit	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	V <sub>LL</sub>	V <sub>R</sub> *	Gnd	
-	150	μAdc	2	-	3	12	11	-	12	4, 13	
-	150	↓	3	-	-	12	↓	-	12	2, 4, 13	
-	270		12	-	-	-		-	-	2, 3, 4, 13	
-	270		12	-	3	-		-	-	2, 4, 13	
-	150		13	-	-	12		↓	-	12	2, 3, 4
420	-	μAdc	1	12	3, 13	2	11		-	-	4
↓	-	↓	1	-	13	2, 12	↓		-	12	3, 4
	-		14	12	2	13			-	-	3, 4
	-		14	3	2	12, 13		↓	-	12	4
	-		-	-	-	-			-	-	-
-	320	mVdc	-	2	12, 13	-	11		-	-	3, 4
↓	↓	↓	-	14	12	-	-		-	-	2, 3, 4, 13
			-	13	2, 12	-	-	-	-	3, 4	
			-	1	12	-	↓	-	-	2, 3, 4, 13	
-	320	mVdc	-	3	13	12		11	-	12	2, 4
320	mVdc	-	-	2	3, 12	11		-	12	4, 13	
-	-	μAdc	-	-	-	-		-	11	-	2, 3, 4, 12, 13

Characteristic	Symbol	Pin Under Test	MC878P Test Limits								MC778P Test Limits								TEST VOLTAGE APPLIED TO PINS LISTED BELOW:							
			0°C		+25°C		+75°C		Unit		+15°C		+25°C		+55°C		Unit									
			Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max			V <sub>in</sub>	V <sub>on</sub>	V <sub>bot</sub>	V <sub>off</sub>	V <sub>cc</sub>	V <sub>ll</sub>	V <sub>R</sub> *	Gnd
Input Current	I <sub>in</sub>	2	-	150	-	140	-	140	$\mu$ A <sub>dc</sub>	-	150	-	150	-	150	$\mu$ A <sub>dc</sub>	-	2	-	3	12	11	-	-	12	4, 13
	I <sub>in</sub>	3	-	150	-	140	-	140	$\mu$ A <sub>dc</sub>	-	150	-	150	-	150	$\mu$ A <sub>dc</sub>	-	3	-	-	12	-	-	-	12	2, 4, 13
	1.8 I <sub>in</sub>	12	-	270	-	250	-	250	$\mu$ A <sub>dc</sub>	-	270	-	270	-	270	$\mu$ A <sub>dc</sub>	-	12	-	-	-	-	-	-	-	2, 3, 4, 13
	1.8 I <sub>in</sub>	12	-	270	-	250	-	250	$\mu$ A <sub>dc</sub>	-	270	-	270	-	270	$\mu$ A <sub>dc</sub>	-	12	-	3	-	-	-	-	-	2, 4, 13
	I <sub>in</sub>	13	-	150	-	140	-	140	$\mu$ A <sub>dc</sub>	-	150	-	150	-	150	$\mu$ A <sub>dc</sub>	-	13	-	-	12	-	-	-	12	2, 3, 4
Output Current	I <sub>A3</sub>	1	420	-	430	-	395	-	$\mu$ A <sub>dc</sub>	420	-	420	-	420	-	$\mu$ A <sub>dc</sub>	1	12	3, 13	2	11	-	-	-	-	4
	I <sub>A3</sub>	1	-	-	-	-	-	-	$\mu$ A <sub>dc</sub>	-	-	-	-	-	-	$\mu$ A <sub>dc</sub>	1	-	13	2, 12	-	-	-	-	12	3, 4
	I <sub>A3</sub>	14	-	-	-	-	-	-	$\mu$ A <sub>dc</sub>	-	-	-	-	-	-	$\mu$ A <sub>dc</sub>	14	12	2	13	-	-	-	-	-	3, 4
	I <sub>A3</sub>	14	-	-	-	-	-	-	$\mu$ A <sub>dc</sub>	-	-	-	-	-	-	$\mu$ A <sub>dc</sub>	14	3	2	12, 13	-	-	-	-	12	4
	I <sub>A3</sub>	14	-	-	-	-	-	-	$\mu$ A <sub>dc</sub>	-	-	-	-	-	-	$\mu$ A <sub>dc</sub>	-	-	-	-	-	-	-	-	-	-
Output Voltage	V <sub>out</sub>	1	-	400	-	350	-	300	mV <sub>dc</sub>	-	400	-	300	-	320	mV <sub>dc</sub>	-	2	12, 13	-	11	-	-	-	-	3, 4
	V <sub>out</sub>	1	-	-	-	-	-	-	mV <sub>dc</sub>	-	-	-	-	-	-	mV <sub>dc</sub>	-	14	12	-	-	-	-	-	-	2, 3, 4, 13
	V <sub>out</sub>	14	-	-	-	-	-	-	mV <sub>dc</sub>	-	-	-	-	-	-	mV <sub>dc</sub>	-	-	13	2, 12	-	-	-	-	-	3, 4
	V <sub>out</sub>	14	-	-	-	-	-	-	mV <sub>dc</sub>	-	-	-	-	-	-	mV <sub>dc</sub>	-	-	1	12	-	-	-	-	-	2, 3, 4, 13
	V <sub>out</sub>	14	-	-	-	-	-	-	mV <sub>dc</sub>	-	-	-	-	-	-	mV <sub>dc</sub>	-	-	-	-	-	-	-	-	-	-
Saturation Voltage	V <sub>CE(sat)</sub>	1	-	250	-	250	-	250	mV <sub>dc</sub>	-	220	-	230	-	320	mV <sub>dc</sub>	-	3	13	12	11	-	-	-	12	2, 4
	V <sub>CE(sat)</sub>	14	-	250	-	250	-	250	mV <sub>dc</sub>	-	220	-	230	-	320	mV <sub>dc</sub>	-	-	2	3, 12	11	-	-	-	12	4, 13
Leakage Current	I <sub>L</sub>	11	-	100	-	100	-	100	$\mu$ A <sub>dc</sub>	-	-	-	-	-	-	$\mu$ A <sub>dc</sub>	-	-	-	-	-	-	11	-	-	2, 3, 4, 12, 13

\* Apply to V<sub>CC</sub> thru resistor prior to applying V<sub>off</sub>. Ground inputs of flip-flop not under test. Other pins not listed are left open.

SWITCHING TIMES  
TEST CIRCUIT AND WAVEFORMS

FIGURE 1

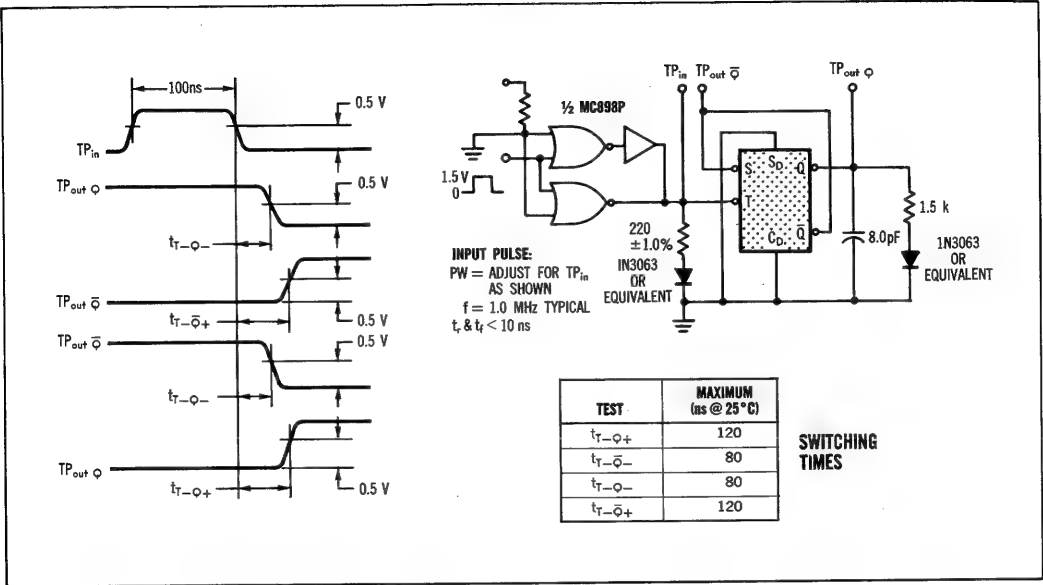


FIGURE 2A — SET-UP AND RELEASE TIMES TEST CIRCUIT

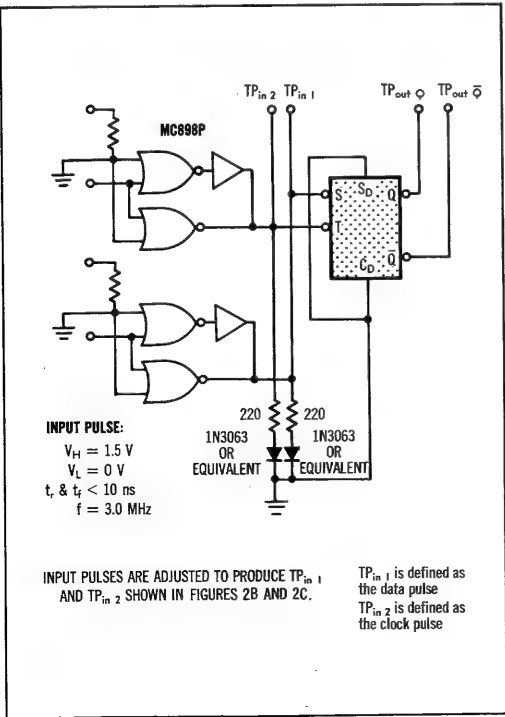


FIGURE 2B — SET-UP TIME WAVEFORMS

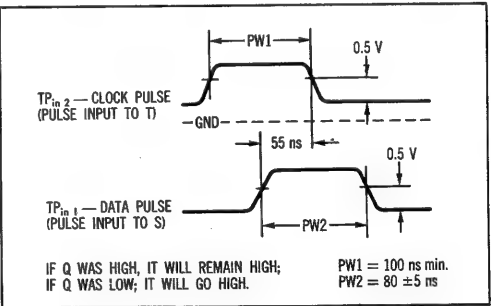
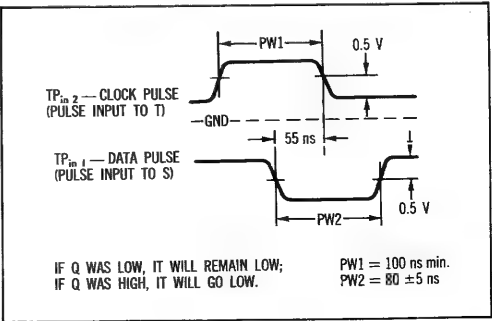


FIGURE 2C — RELEASE TIME WAVEFORMS



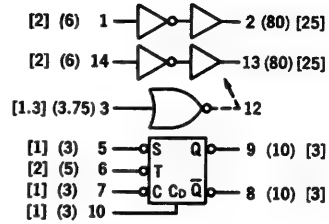
# MULTIFUNCTION DEVICES

# PLASTIC MRTL MC700P/800P series

(1 J-K Flip-Flop, 1 Expander, 2 Buffers)

## MC779P • MC879P

A medium-power monolithic device consisting of one J-K flip-flop, one expander, and two buffer circuits in a single package. This J-K flip-flop can be operated in the toggling mode. Simultaneous logic ONE pulses applied to the SET and CLEAR terminals cause the output state to reverse. A direct clear input allows asynchronous entry for preclearing counters, inserting parallel data into registers, and other similar applications. The MRTL expander is designed to increase the fan-in capability of gates with expander inputs, and the buffers are high fan-out gates with single inputs.



$$2 = \bar{1}$$

$$12 = \bar{3}$$

### CLOCKED INPUT OPERATION ①

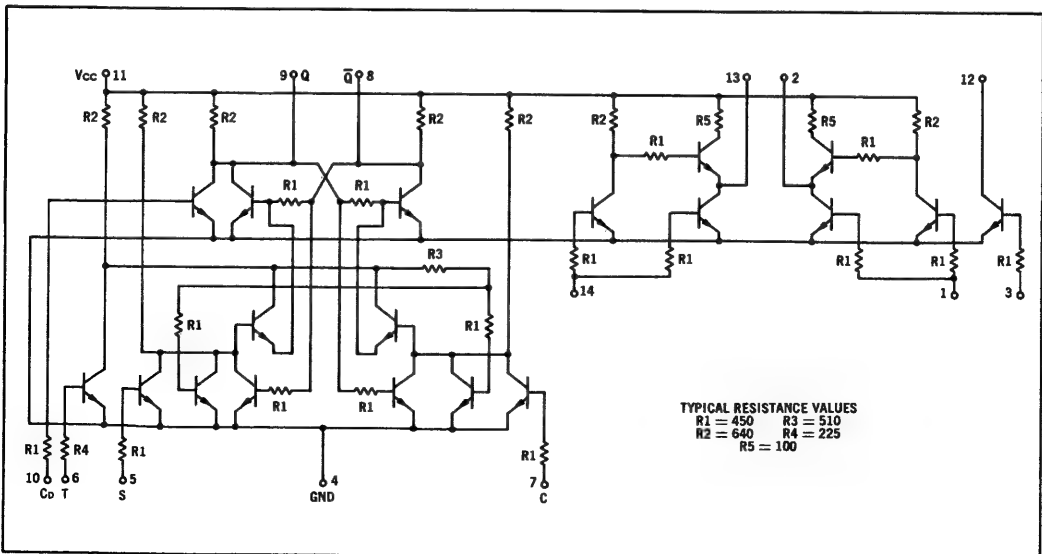
$t_n$ ③	$t_{n+1}$ ③		
S	C	Q	$\bar{Q}$
1	1	$Q_n$ ③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	$Q_n$ ③

	$f_{Tog}$ MHz	$t_{pd}$	$P_D$ (mW)	
			(Inputs High)	(Inputs Low)
FLIP-FLOP	4	—	91½	79
EACH BUFFER	—	15	25	45
EXPANDER	—	12	25	Negligible

(Only Clock Input High)

1. Direct input ( $C_D$ ) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted  $t_n$  and the time period subsequent to this transition is denoted  $t_{n+1}$ .
3.  $Q_n$  is the state of the Q output in the time period  $t_n$ .

NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL  
 NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL



## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC879P Test Limits								MC779P Test Limits								TEST VOLTAGE							Gnd
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	APPLIED TO PINS LISTED BELOW:									
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		V <sub>IN</sub>	V <sub>ON</sub>	V <sub>BOT</sub>	V <sub>OFF</sub>	V <sub>CC</sub>	V <sub>R</sub> *				
Input Current	2I <sub>in</sub>	1	-	1200	-	1200	-	1140	μA <sub>dc</sub>	-	1000	-	1000	-	940	μA <sub>dc</sub>	1	-	-	-	11	2	3,4,5,6,7,10,14			
	I <sub>in</sub>	3	-	600	-	600	-	570	↓	-	500	-	500	-	470	↓	3	-	-	-	12	1,4,5,6,7,10,14				
	I <sub>in</sub>	5	-	600	-	600	-	570	-	-	500	-	500	-	470	-	5	-	8	-	-	1,3,4,14				
	2I <sub>in</sub>	6	-	1200	-	1200	-	1140	-	-	1000	-	1000	-	940	-	6	-	5,7	-	-	↓				
	I <sub>in</sub>	7	-	600	-	600	-	570	-	-	500	-	500	-	470	-	7	-	9	-	-	-				
	I <sub>in</sub>	10	-	600	-	600	-	570	-	-	500	-	500	-	470	-	10	-	8	-	-	-				
	2I <sub>in</sub>	14	-	1200	-	1200	-	1140	↓	-	1000	-	1000	-	940	↓	14	-	-	-	↓	13	1,3,4,5,6,7,10			
Output Current	I <sub>AB</sub>	2	15.0	-	15.0	-	14.25	-	mA <sub>dc</sub>	13.50	-	13.75	-	12.50	-	mA <sub>dc</sub>	-	2	-	1	11	-	3,4,5,6,7,10,14			
	I <sub>A3</sub>	8	1.8	-	1.8	-	1.71	-	↓	1.65	-	1.65	-	1.56	-	↓	-	8	5,10	-	-	-	1,3,4,14			
	I <sub>A3</sub>	8	-	-	-	-	-	-	↓	-	-	-	-	-	-	↓	-	8,10	5	-	-	↓				
	I <sub>A3</sub>	9##	↓	-	↓	-	↓	-	-	2.65	-	2.65	-	2.50	-	↓	-	-	7	10	-	-	1,3,4,14			
	I <sub>A5</sub>	12	3.0	-	3.0	-	2.85	-	↓	2.65	-	2.65	-	2.50	-	↓	-	12	-	3	12	-	1,4,5,6,7,10,14			
	I <sub>AB</sub>	13	15.0	-	15.0	-	14.25	-	↓	13.50	-	13.75	-	12.50	-	↓	-	13	-	14	↓	-	1,3,4,5,6,7,10			
Output Voltage	V <sub>out</sub>	2	-	500	-	400	-	400	mV <sub>dc</sub>	-	400	-	300	-	320	mV <sub>dc</sub>	-	1	-	-	11	2	3,4,5,6,7,10,14			
	8Δ##	-	-	↓	-	↓	-	↓	-	-	-	-	-	-	-	-	-	5,7	-	-	-	-	1,3,4,10,14			
	8Δ**	-	-	↓	-	↓	-	↓	-	-	-	-	-	-	-	-	-	5	-	7	-	-	↓			
	8Δ**	-	-	↓	-	↓	-	↓	-	-	-	-	-	-	-	-	-	-	-	5,7	-	-	1,3,4,8,14			
	9	-	-	↓	-	↓	-	↓	-	-	-	-	-	-	-	-	-	10	-	-	-	-	1,3,4,10,14			
	9Δ**	-	-	↓	-	↓	-	↓	-	-	-	-	-	-	-	-	-	5,7	-	-	-	-	↓			
	9Δ##	-	-	↓	-	↓	-	↓	-	-	-	-	-	-	-	-	-	7	-	5	-	-	1,3,4,14			
	9Δ##	-	-	↓	-	↓	-	↓	-	-	-	-	-	-	-	-	-	-	-	5,7	-	-	↓			
	12	-	-	↓	-	↓	-	↓	-	-	-	-	-	-	-	-	-	3	-	-	12	-	1,4,5,6,7,10,14			
	13	-	-	↓	-	↓	-	↓	-	-	-	-	-	-	-	-	-	14	-	-	13	-	1,3,4,5,6,7,10			
Saturation Voltage	V <sub>CE(sat)</sub>	2	-	400	-	300	-	350	mV <sub>dc</sub>	-	300	-	290	-	320	mV <sub>dc</sub>	-	-	1	-	11	2	3,4,5,6,7,10,14			
	8##	-	-	↓	-	↓	-	↓	-	-	-	-	-	-	-	-	-	-	10	-	-	-	1,3,4,14			
	9	-	-	↓	-	↓	-	↓	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1,3,4,8,14			
	9**	-	-	↓	-	↓	-	↓	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1,3,4,14			
	12	-	-	↓	-	↓	-	↓	-	-	-	-	-	-	-	-	-	-	3	-	12	-	1,4,5,6,7,10,14			
	13	-	-	↓	-	↓	-	↓	-	-	-	-	-	-	-	-	-	-	14	-	13	-	1,3,4,5,6,7,10			
Switching Time	t	1+2-	-	-	-	30	-	-	ns	-	-	-	30	-	-	ns	Pulse In	Pulse Out	-	-	11	-	3,4,14			
		1-2+	-	-	-	45	-	-	↓	-	-	-	45	-	-	↓	1	2	-	-	-	-	3,4,14			
		14+13-	-	-	-	30	-	-	↓	-	-	-	30	-	-	↓	14	13	-	-	-	-	1,3,4			
		14-13+	-	-	-	45	-	-	↓	-	-	-	45	-	-	↓	14	13	-	-	-	-	1,3,4			
			-	-	-	-	-	-	↓	-	-	-	-	-	-	↓										

Pins not listed are left open.

 ## Pin 8 = LOW } Set by a momentary ground prior to the application  
 \*\* Pin 9 = LOW } of the negative-going clock pulse.

Δ = Clock Pulse to pin 6, see Figure 1.

\* = Resistor value to V<sub>CC</sub>.

FIGURE 1—CLOCK PULSE DEFINITION

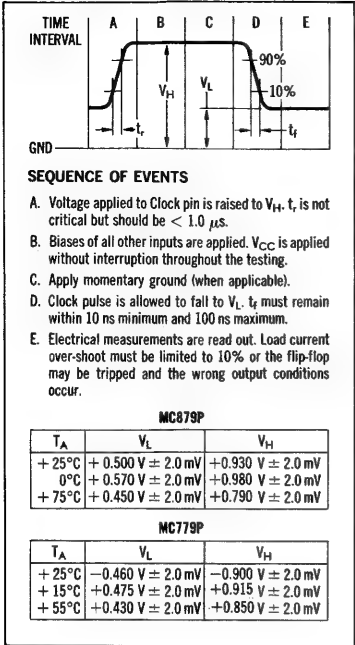


FIGURE 2—TOGGLE MODE TEST CIRCUIT

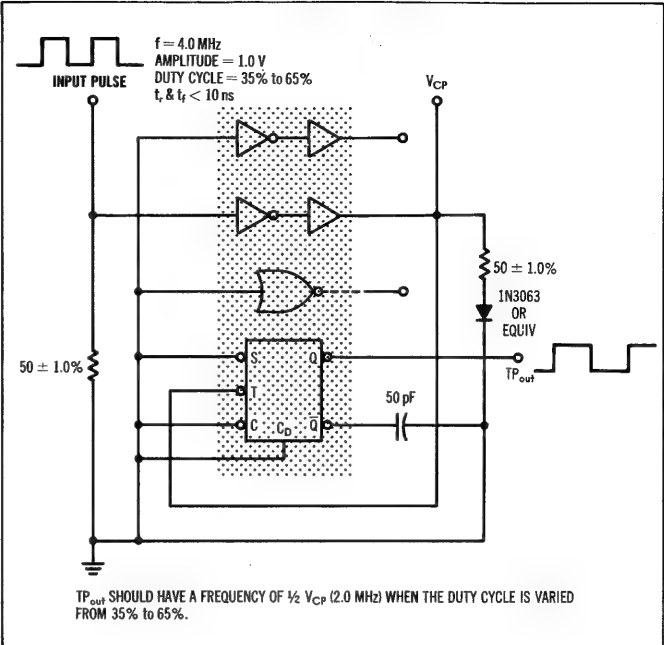
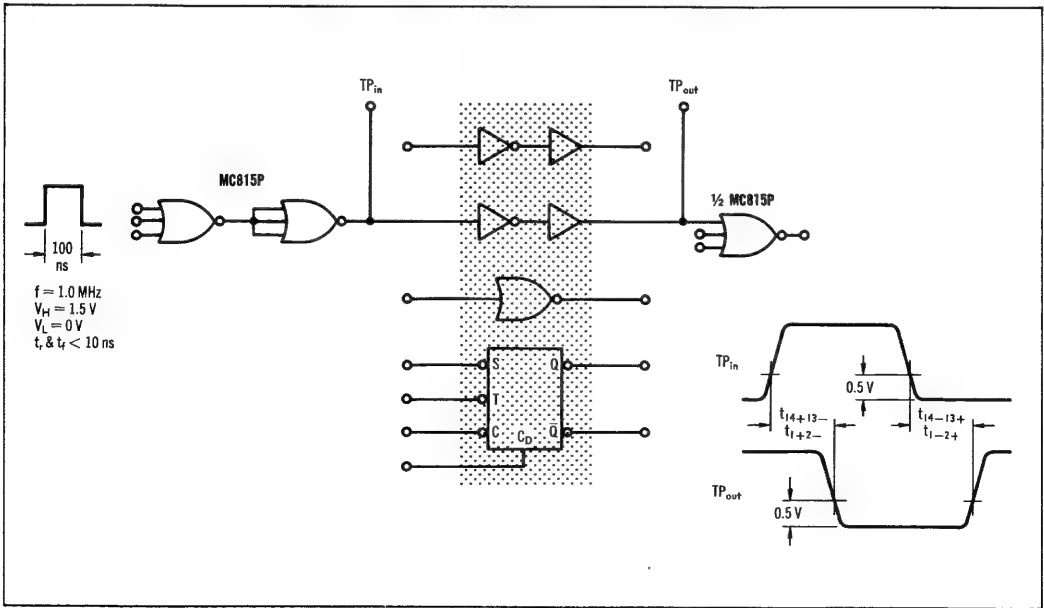


FIGURE 3—SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



# DECADE UP COUNTER

## PLASTIC MRTL MC700P/800P series

### MC780P • MC880P

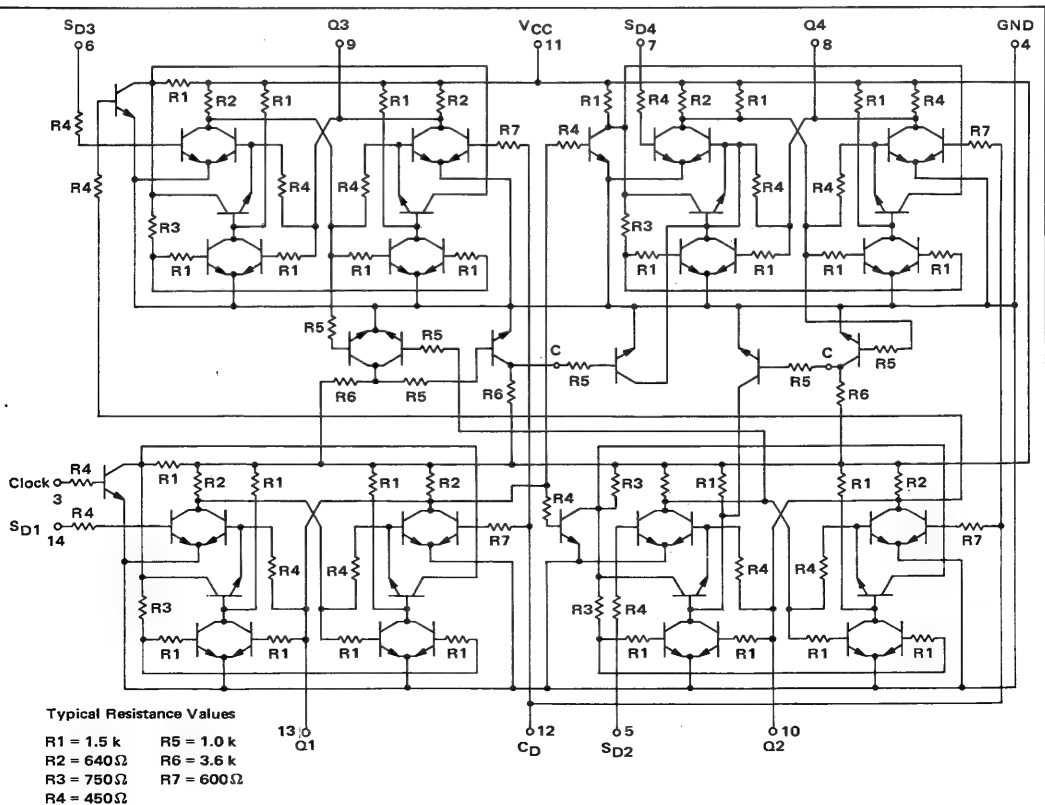
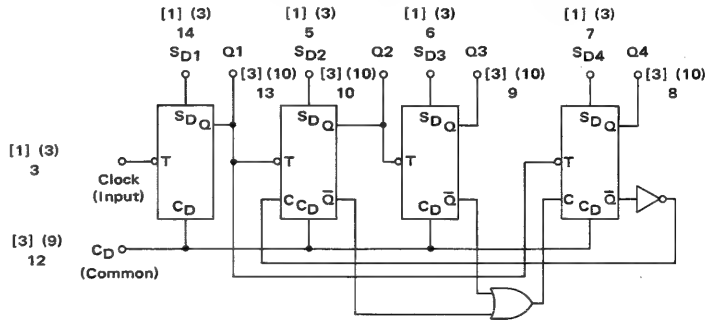
#### DECODING LOGIC

	$\bar{A}$	$\bar{B}$	$\bar{C}$	$\bar{D}$
0	A	B	C	D
1	A	B	C	$\bar{D}$
2	A	$\bar{B}$	C	D
3	A	$\bar{B}$	C	$\bar{D}$
4	A	B	$\bar{C}$	D
5	A	B	$\bar{C}$	$\bar{D}$
6	A	$\bar{B}$	$\bar{C}$	D
7	A	$\bar{B}$	$\bar{C}$	$\bar{D}$
8	$\bar{A}$	B	C	D
9	$\bar{A}$	B	C	$\bar{D}$

$P_D = 250 \text{ mW typ}$   
 $f = 4.0 \text{ MHz}$   
 Counting Frequency

The MC780P/MC880P is a monolithic decade up counter consisting of four flip-flops internally interconnected. A common direct clear is provided to return all outputs to the logical zero level. Individual direct set inputs are provided to set the counter to any specific count.

Number in parenthesis indicates loading factor for mW MRTL.  
 Number in brackets indicates loading factor for MRTL.





# ELECTRICAL CHARACTERISTICS

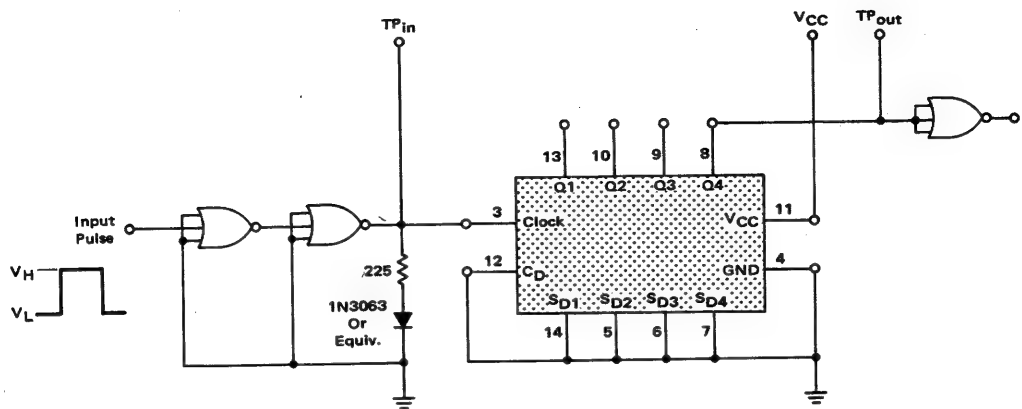
ELECTRICAL CHARACTERISTICS																	TEST VOLTAGE VALUES					Gnd
																	(Volts)					
																	V <sub>In</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	
																	@ Test Temperature					
																	MC880P					
																	0°C	+25°C	+75°C	+15°C	+25°C	+55°C
																	MC780P					
																	+25°C	+55°C	+25°C	+55°C	+25°C	+55°C
																	TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					
Characteristic	Symbol	Pin Under Test	MC880P Test Limits						MC780P Test Limits						TEST VOLTAGE APPLIED TO PINS LISTED BELOW:							
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	V <sub>In</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	
Input Current	I <sub>In</sub>	3	-	600	-	600	-	570	μA <sub>dc</sub>	-	500	-	500	-	470	μA <sub>dc</sub>	3	-	-	-	11	4
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	5	-	-	-	↓	↓
		6	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	6	-	-	-	↓	↓
		7	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	7	-	-	-	↓	↓
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	14	-	-	-	↓	↓
3 I <sub>In</sub>	12	-	1800	-	1800	-	710	↓	-	1500	-	1500	-	1410	↓	12	-	-	-	↓	↓	
Output Current	I <sub>A3</sub>	8	-1.80	-	-1.80	-	-1.71	-	mA <sub>dc</sub>	-1.65	-	-1.65	-	-1.56	-	mA <sub>dc</sub>	-	8	7	-	11	4
		9	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	↓	↓	9	6	-	↓	↓	
		10	-	-	-	-	-	-	↓	-	-	-	-	-	-	↓	-	10	5	-	↓	↓
		13	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	13	14	-	↓	↓
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	↓	↓
Output Voltage	V <sub>out</sub> *	8	-	500	-	400	-	400	mV <sub>dc</sub>	-	400	-	300	-	320	mV <sub>dc</sub>	-	-	-	-	11	4
		9	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	↓	↓
		10	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	↓	↓
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	↓	↓
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	↓	↓
Saturation Voltage	V <sub>CE(sat)</sub>	8	-	400	-	300	-	350	mV <sub>dc</sub>	-	300	-	290	-	320	mV <sub>dc</sub>	-	-	12	-	11	4
		9	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	↓	-	↓	↓
		10	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	↓	-	↓	↓
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	↓	-	↓	↓
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	↓	-	↓	↓
Power Supply Current Drain	I <sub>PD</sub>	11	-	-	-	75	-	-	mA <sub>dc</sub>	-	-	-	75	-	-	mA <sub>dc</sub>	-	-	-	-	11	4
		11	-	-	-	75	-	-	↓	-	-	-	75	-	-	↓	-	-	-	-	11	4
		11	-	-	-	75	-	-	↓	-	-	-	75	-	-	↓	-	-	-	-	11	4
		11	-	-	-	75	-	-	↓	-	-	-	75	-	-	↓	-	-	-	-	11	4
		11	-	-	-	75	-	-	↓	-	-	-	75	-	-	↓	-	-	-	-	11	4
Switching Times Propagation Delay	t <sub>3-8+</sub>	8	-	-	-	100	-	-	ns	-	-	-	100	-	-	ns	Pulse In	Pulse Out	-	-	11	4
		8	-	-	-	75	-	-	ns	-	-	-	75	-	-	ns	3	8	-	-	11	4
		8	-	-	-	75	-	-	ns	-	-	-	75	-	-	ns	3	8	-	-	11	4
		8	-	-	-	75	-	-	ns	-	-	-	75	-	-	ns	3	8	-	-	11	4
		8	-	-	-	75	-	-	ns	-	-	-	75	-	-	ns	3	8	-	-	11	4

Pins not listed are left open.

\*Apply momentary ground to pin under test prior to measurement of V<sub>out</sub> on that pin.

MC780P, MC880P (continued)

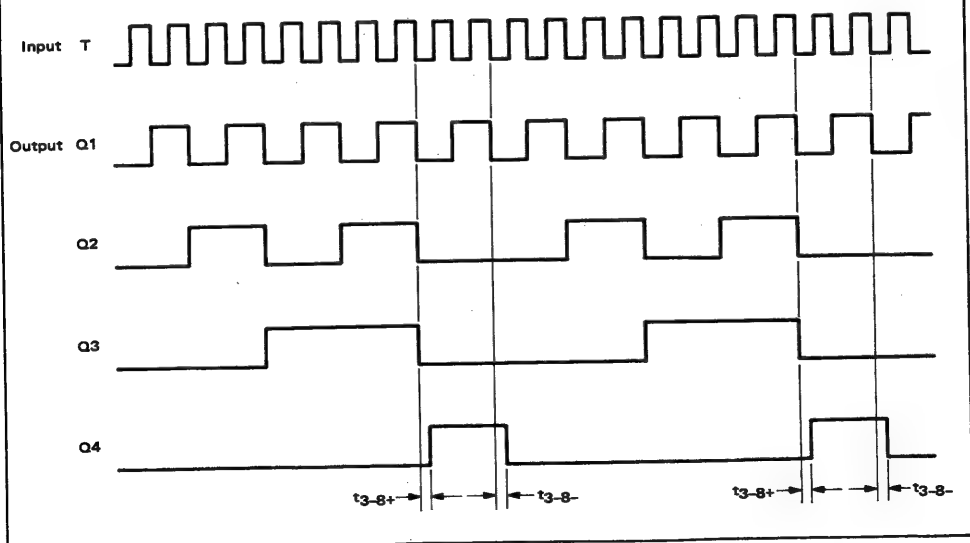
SWITCHING TIME TEST CIRCUIT



$V_L = 0$   
 $V_H = 1.0\text{ V}$   
Pulse Width = 100 ns  
PRF = 1.0 MHz Typ

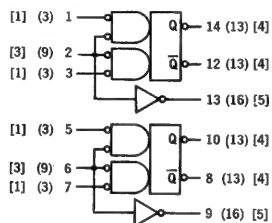
Any MRTL 3-input gates may be used as load and driving gates.

VOLTAGE WAVEFORMS AND DEFINITIONS



**MC783P • MC883P**

Dual half-shift registers each with built-in inverter, in a single package. Information coming in on pins 1 and 2 will be transferred to pins 14 and 12 when the gating signal, pin 3, goes low. If all three inputs, 1, 2, and 3, are low, the outputs, 12 and 14, will both be low.



$$14 = \overline{12} (1 + 2)$$

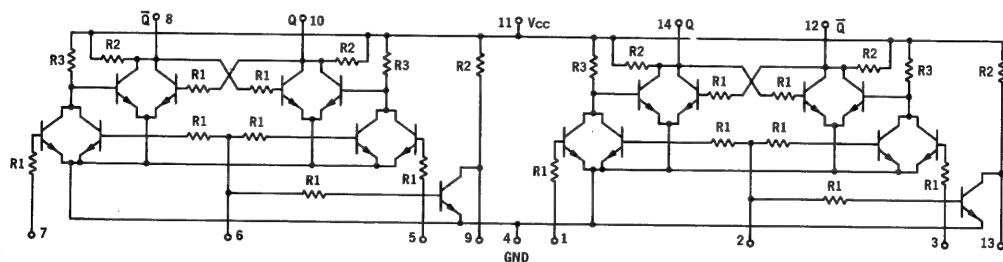
$$12 = \overline{14} (3 + 2)$$

$$t_{pd} = 22 \text{ ns typ}$$

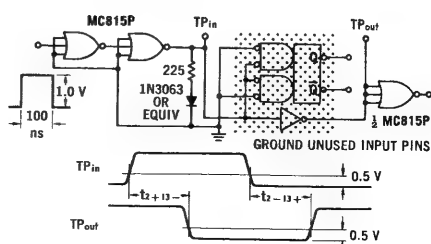
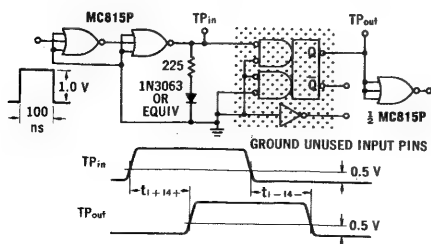
$$P_D = 140 \text{ mW typ}$$

NUMBER IN PARENTHESES INDICATES  
LOADING FACTOR FOR mW MRTL

NUMBER IN BRACKETS INDICATES  
LOADING FACTOR FOR MRTL



TYPICAL RESISTANCE  
VALUES  
R1 = 450 Ω  
R2 = 640 Ω  
R3 = 800 Ω

**SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS**

Test procedures are shown for one half-shift register only. The other half-shift register is tested in the same manner.

Test procedures are shown for one half-shift register only. The other half-shift register is tested in the same manner.

		TEST VOLTAGE VALUES						
		(Volts)						
		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>		
MC883P	0°C	0.960	0.930	1.80	0.570	3.60		
	+25°C	0.910	0.880	1.80	0.500	3.60		
	+75°C	0.820	0.790	1.80	0.450	3.60		
MC783P	+15°C	0.865	0.865	1.80	0.475	3.60		
	+25°C	0.850	0.850	1.80	0.460	3.60		
	+55°C	0.800	0.800	1.80	0.430	3.60		
Test Limits		TEST VOLTAGE APPLIED TO PINS LISTED BELOW:						
+55°C		Unit	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	Gnd
Min	Max							
-	470	μA <sub>dc</sub>	1	-	2	-	11	4
-	1410	↓	2	-	1, 3	-	↓	↓
-	470		3	-	2	-		
2.03	-	mA <sub>dc</sub>	-	2, 12	-	-	11	4, 14↑
2.03	-	↓	-	3, 12	-	-	↓	4
2.5	-		-	13	-	2		4
2.03	-	↓	-	2, 14	-	-	↓	4, 12↑
2.03	-		-	1, 14	-	-		4
-	320	mV <sub>dc</sub>	-	14	2, 3	-	11	4
-	↓	↓	-	2	-	-	↓	↓
-			-	12	1, 2	-		
-	320	mV <sub>dc</sub>	-	-	1, 2, 3	-	11	4, 12↑
-	↓	↓	-	-	2	2, 3	↓	4, 14
-			-	-	1, 2, 3	-		4
-	↓	↓	-	-	-	1, 2	↓	4, 14↑
-			-	-	-	-		4, 12
-	-	ns	Pulse In	Pulse Out				
-	-	↓	2	13	-	-	11	4
-	-		2	13	-	-	↓	4
-	-		1	14	-	-		4, 12
-	-		1	14	-	-		4, 12

Ground input pins of half-shift register not under test. Other pins not listed are left open.

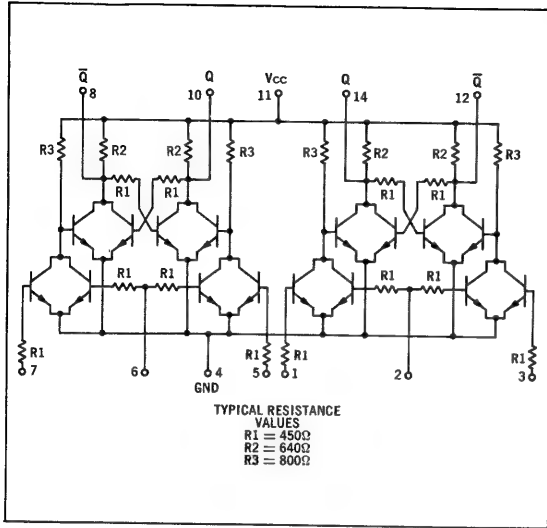
† Silicon diode to ground.

**MC783P, MC883P (continued)**

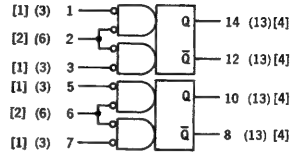
# DUAL HALF-SHIFT REGISTER

PLASTIC MRTL MC700P/800P series

## MC784P • MC884P



Two half-shift registers in a single package. Each is a bistable storage element. E.g., information coming in on pins 1 and 3 will be transferred to pins 14 and 12 when the gating signal, pin 2, goes low. If all three inputs, 1, 2, and 3, are low, the outputs, 14 and 12, will both be low.



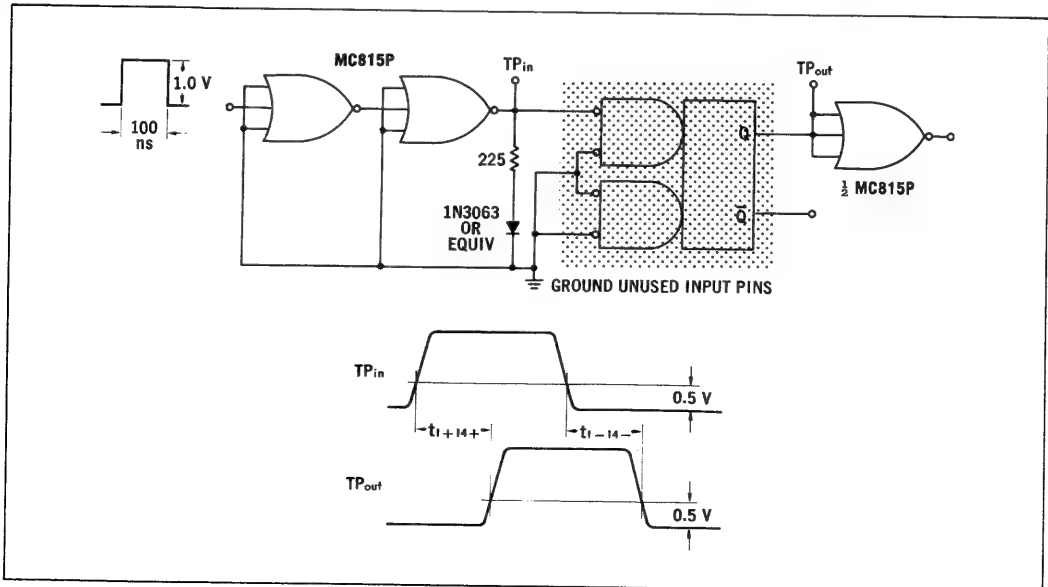
NUMBER IN PARENTHESIS INDICATES mW MRTL LOADING FACTOR

NUMBER IN BRACKETS INDICATES MRTL LOADING FACTOR

$t_{pd} = 22 \text{ ns typ}$

$P_o = 120 \text{ mW typ}$

## SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



## ELECTRICAL CHARACTERISTICS

Test procedures are shown for one half-shift register only.  
The other half-shift register is tested in the same manner.

		TEST VOLTAGE VALUES							
		(Volts)							
		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>			
MC884P	0°C	0.960	0.930	1.80	0.570	3.60			
	+25°C	0.910	0.880	1.80	0.500	3.60			
	+75°C	0.820	0.790	1.80	0.450	3.60			
MC784P	+15°C	0.865	0.865	1.80	0.475	3.60			
	+25°C	0.850	0.850	1.80	0.460	3.60			
	+55°C	0.800	0.800	1.80	0.430	3.60			
st Limits			TEST VOLTAGE						
+55°C		Unit	APPLIED TO PINS LISTED BELOW:						
Min	Max		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	Gnd	
-	470	μA dc	1	-	2	-	11	4	
-	940	↓	2	-	1, 3	-	↓	↓	
-	470		3	-	2	-			
2.03	-	mA dc	-	2, 12	-	-	11	4, 14	
↓	-	↓	-	3, 12	-	-	-	4	
-	-		-	2, 14	-	-	↓	4, 12	
-	-		-	1, 14	-	-		4	
-	320	mV dc	-	14	2, 3	-	11	4	
-	320	mV dc	-	12	1, 2	-	11	4	
-	320	mV dc	-	-	1, 2, 3	-	11	4, 12	
-	↓	↓	-	-	-	2, 3	↓	4, 14	
-			-	-	1, 2, 3	-		4, 14	
-			-	-	-	1, 2	↓	4	
			Pulse In	Pulse Out					
-	-	ns	1	14	-	-	11	4, 12	
-	-	ns	1	14			11	4, 12	

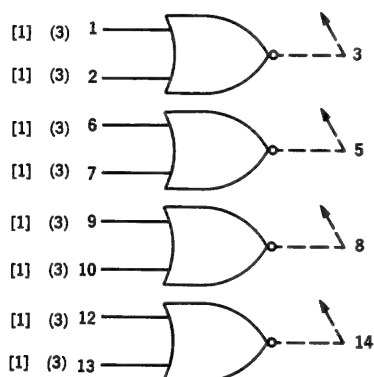
Characteristic	Symbol	Pin Under Test	MC884P Test Limits							MC784P Test Limits							TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					Gnd
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	V <sub>in</sub>	V <sub>on</sub>	V <sub>BoT</sub>	V <sub>off</sub>	V <sub>Cc</sub>	
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max							
Input Current	I <sub>in</sub>	1	-	600	-	600	-	570	μA <sub>dc</sub>	-	500	-	500	-	470	μA <sub>dc</sub>	1	-	2	-	11	4
	2I <sub>in</sub>	2	-	1200	-	1200	-	1140	↓	-	1000	-	1000	-	940	↓	2	-	1, 3	-	↓	↓
	I <sub>in</sub>	3	-	600	-	600	-	570	↓	-	500	-	500	-	470	↓	3	-	2	-	↓	↓
Output Current	I <sub>A4</sub>	12	2.4	-	2.4	-	2.28	-	mA <sub>dc</sub>	2.15	-	2.15	-	2.03	-	mA <sub>dc</sub>	-	-	2, 12	-	11	4, 14†
		12	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	-	3, 12	-	-	4	
		14	-	-	-	-	-	-	↓	-	-	-	-	↓	-	↓	-	-	2, 14	-	↓	4, 12†
		14	↓	-	↓	-	↓	-	↓	-	-	-	-	↓	-	↓	-	-	1, 14	-	↓	4
Output Voltage	V <sub>out</sub>	12	-	500	-	400	-	400	mV <sub>dc</sub>	-	400	-	300	-	320	mV <sub>dc</sub>	-	14	2, 3	-	11	4
		14	-	500	-	400	-	400	mV <sub>dc</sub>	-	400	-	300	-	320	mV <sub>dc</sub>	-	12	1, 2	-	11	4
Saturation Voltage	V <sub>CE(sat)</sub>	12	-	400	-	300	-	350	mV <sub>dc</sub>	-	300	-	290	-	320	mV <sub>dc</sub>	-	-	1, 2, 3	-	11	4, 12†
		12	-	-	-	-	-	-	↓	-	-	-	-	-	-	↓	-	-	-	2, 3	↓	4, 14
		14	-	-	-	-	-	-	↓	-	-	-	-	-	-	↓	-	-	1, 2, 3	-	↓	4, 14†
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1, 2	↓	4
Switching Time	t	1+14+ 1-14-	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	Pulse In	Pulse Out	-	-	11	4, 12
			-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	1	14	-	-	11	4, 12

Ground input pins of half-register not under test. Other pins not listed are left open.

† Silicon diode to ground.

**MC785P • MC885P**

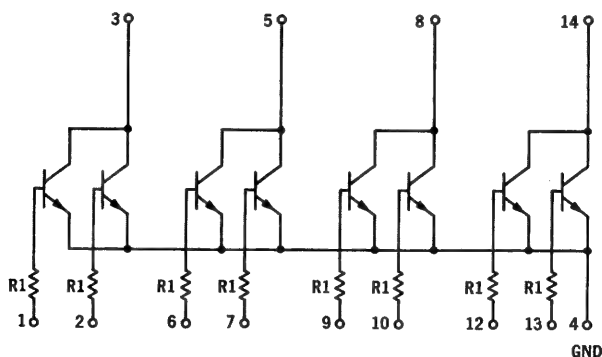
Four 2-input expanders housed in a single package increase the input capability of MRTL gates.



$$3 = 1 + 2$$

$t_{pd} = 12 \text{ ns}$   
 $P_d = 20 \text{ mW (Input High)}$   
 Negligible (Inputs Low)

NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL  
 NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL  
 SEE GENERAL INFORMATION SECTION FOR EXPANDER RULES



$V_{cc}$  CONNECTION TO PIN 11 IS NOT SHOWN

TYPICAL RESISTANCE  
 VALUES  
 $R1 = 450 \Omega$

## ELECTRICAL CHARACTERISTICS

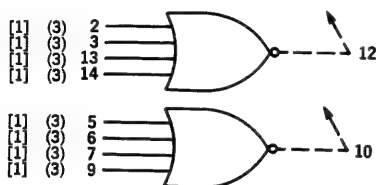
Test procedures are shown for one expander only.  
The other expanders are tested in the same manner.

		TEST VOLTAGE VALUES																			
		(Volts)										(Ohms)									
		V <sub>IN</sub>	V <sub>ON</sub>	V <sub>BOT</sub>	V <sub>OFF</sub>	V <sub>CC</sub>	V <sub>R</sub> *														
MC885P		Temperature		@ Test																	



**MC786P • MC886P**

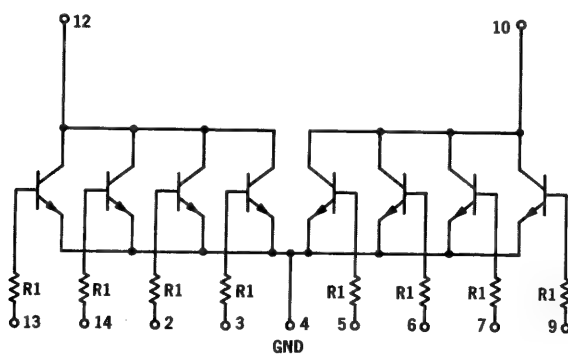
Two 4-input gate expanders housed in a single package. Each may be used independently or combined. Each expander increases the input capability of a standard MRTL gate by four.



$$12 = \overline{2 + 3 + 13 + 14}$$

$t_{pd} = 12 \text{ ns}$   
 $P_D = 20 \text{ mW}$  (Input High)  
 Negligible (Inputs Low)

NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL  
 NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL  
 SEE GENERAL INFORMATION SECTION FOR EXPANDER RULES



$V_{CC}$  CONNECTION TO PIN 11 NOT SHOWN

TYPICAL RESISTANCE  
 VALUES  
 $R1 = 450 \Omega$

## ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.  
The other expander is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES						
		(Volts)					(Ohms)	
		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	V <sub>R</sub> *	
MC886P	0°C	0.960	0.930	1.80	0.570	3.60	640	
	+25°C	0.910	0.880	1.80	0.500	3.60	640	
	+75°C	0.820	0.790	1.80	0.450	3.60	750	
MC786P	+15°C	0.865	0.865	1.80	0.475	3.60	640	
	+25°C	0.850	0.850	1.80	0.460	3.60	640	
	+55°C	0.800	0.800	1.80	0.430	3.60	640	

Characteristic	Symbol	Pin Under Test	MC886P Test Limits								MC786P Test Limits								TEST VOLTAGE APPLIED TO PINS LISTED BELOW:						Gnd
			0°C		+25°C		+75°C		Unit		+15°C		+25°C		+55°C		Unit		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	V <sub>R</sub> *	
			Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max									
Input Current	I <sub>in</sub>	2 3 13 14	-	600	-	600	-	570	μA <sub>dc</sub>		-	500	-	500	-	470	μA <sub>dc</sub>		2 3 13 14	-	3,13,14 2,13,14 2,3,14 2,3,13	-	11	12	4
Output Leakage Current	I <sub>CEX</sub>	12	-	200	-	200	-	250	μA <sub>dc</sub>		-	225	-	225	-	250	μA <sub>dc</sub>		12	-	-	2, 3, 13, 14	11	-	4
Output Voltage	V <sub>out</sub>	12 12 12 12	-	500	-	400	-	400	mV <sub>dc</sub>		-	400	-	300	-	320	mV <sub>dc</sub>		-	13 14 2 3	-	-	11	12	2,3,4,14 2,3,4,13 3,4,13,14 2,4,13,14
Saturation Voltage	V <sub>CE(sat)</sub>	12 12 12 12	-	400	-	300	-	350	mV <sub>dc</sub>		-	300	-	290	-	320	mV <sub>dc</sub>		-	-	13 14 2 3	-	11	12	2,3,4,14 2,3,4,13 3,4,13,14 2,4,13,14

Ground unused input pins. Other pins not listed are left open.

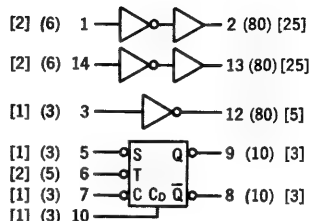
# MULTIFUNCTION DEVICES

# PLASTIC MRTL MC700P/800P series

(1 J-K Flip-Flop, 1 Inverter, 2 Buffers)

## MC787P • MC887P

A medium-power monolithic device consisting of one J-K flip-flop, one inverter, and two buffer circuits in a single package. This J-K flip-flop can be operated in the toggling mode. Simultaneous logic ONE pulses applied to the SET and CLEAR terminals cause the output state to reverse. A direct clear input allows asynchronous entry for pre-clearing counters, inserting parallel data into registers, and other similar applications. The inverter is a basic MRTL gate and the buffers are high fan-out gates with single inputs.



### CLOCKED INPUT OPERATION ①

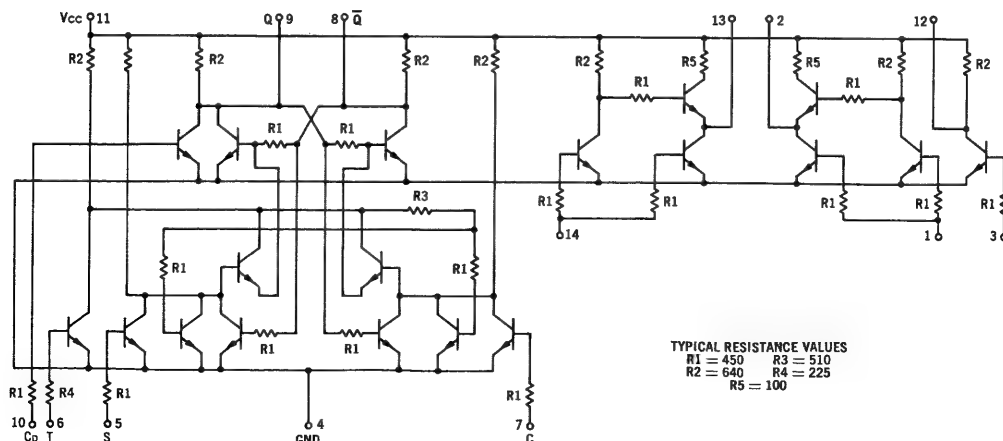
$t_n$ ②		$t_{n+1}$ ③	
S	C	Q	$\bar{Q}$
1	1	$Q_n$ ③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	$Q_n$ ③

	$f_{reg}$ MHz	$t_{pd}$ ns	$P_D$ (mW)	
			(Input High)	(Inputs Low)
FLIP-FLOP	4	—	91‡	79
EACH BUFFER	—	15	25	45
INVERTER	—	12	22	8

‡Only Clock Input High

1. Direct input ( $C_0$ ) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted  $t_n$  and the time period subsequent to this transition is denoted  $t_{n+1}$ .
3.  $Q_n$  is the state of the Q output in the time period  $t_n$ .

NUMBER IN PARENTHESES INDICATES mW MRTL LOADING FACTOR  
NUMBER IN BRACKETS INDICATES MRTL LOADING FACTOR



TYPICAL RESISTANCE VALUES  
R1 = 450 R3 = 510  
R2 = 640 R4 = 225  
R5 = 100

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC887P Test Limits							MC878P Test Limits							TEST VOLTAGE							Gnd	
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	APPLIED TO PINS LISTED BELOW:								
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	V <sub>R</sub> *			
Input Current	2I <sub>in</sub>	1	-	1200	-	1200	-	1140	μA dc	-	1000	-	1000	-	940	μA dc	1	-	-	-	11	2	3,4,5,6,7,10,14		
	I <sub>in</sub>	3	-	600	-	600	-	570	↓	-	500	-	500	-	470	↓	3	-	-	-	-	-	1,4,5,6,7,10,14		
	I <sub>in</sub>	5	-	600	-	600	-	570		-	500	-	500	-	470		5	-	8	-	-	-	1,3,4,14		
	2I <sub>in</sub>	6	-	1200	-	1200	-	1140		-	1000	-	1000	-	940		6	-	5,7	-	-	-	↓		
	I <sub>in</sub>	7	-	600	-	600	-	570		-	500	-	500	-	470		7	-	9	-	-	-			
	I <sub>in</sub>	10	-	600	-	600	-	570		-	500	-	500	-	470		10	-	8	-	-	-			
	2I <sub>in</sub>	14	-	1200	-	1200	-	1140		-	1000	-	1000	-	940		14	-	-	-	↓	13		1,3,4,5,6,7,10	
Output Current	I <sub>AB</sub>	2	15.0	-	15.0	-	14.25	-	mA dc	13.50	-	13.75	-	12.50	-	mA dc	-	8	-	1	11	-	3,4,5,6,7,10,14		
	I <sub>A3</sub>	8	1.8	-	1.8	-	1.71	-	↓	1.65	-	1.65	-	1.56	-	↓	-	8,10	5,10	-	-	-	1,3,4,14		
	I <sub>A3</sub>	9##	-	-	-	-	-	-		-	-	-	-	-	-		-	9	7	10	-	-	↓		
	I <sub>A3</sub>	12	3.0	-	3.0	-	2.85	-		2.65	-	2.65	-	2.50	-		2.50	12	-	3	-	-		1,4,5,6,7,10,14	
	I <sub>A5</sub>	13	15.0	-	15.0	-	14.25	-		13.50	-	13.75	-	12.50	-		12.50	13	-	14	-	-		1,3,4,5,6,7,10	
	I <sub>AB</sub>	2	-	500	-	400	-	400		mV dc	-	400	-	300	-		320	mV dc	-	1	-	11		2	3,4,5,6,7,10,14
Output Voltage	V <sub>out</sub>	8Δ##	-	-	-	-	-	-	↓	-	-	-	-	-	-	↓	-	5,7	-	-	-	-	1,3,4,10,14		
	8Δ**	-	-	-	-	-	-	-		-	-	-	-	-	-		-	5	-	-	-	-	-		
	8Δ**	-	-	-	-	-	-	-		-	-	-	-	-	-		-	-	7	5,7	-	-	-		
	9	-	-	-	-	-	-	-		-	-	-	-	-	-		-	-	10	-	-	-	1,3,4,8,14		
	9Δ**	-	-	-	-	-	-	-		-	-	-	-	-	-		-	-	5,7	-	-	-	1,3,4,10,14		
	9Δ##	-	-	-	-	-	-	-		-	-	-	-	-	-		-	-	7	5	-	-	-		
	9Δ##	-	-	-	-	-	-	-		-	-	-	-	-	-		-	-	-	-	5,7	-	-	↓	
	12	-	-	-	-	-	-	-		-	-	-	-	-	-		-	3	-	-	-	-	1,4,5,6,7,10,14		
	13	-	-	-	-	-	-	-		-	-	-	-	-	-		-	-	14	-	-	-	-		1,3,4,5,6,7,10
	Saturation Voltage	V <sub>CE (sat)</sub>	2	-	400	-	300	-		350	mV dc	-	300	-	290		-	320	mV dc	-	-	1	-		11
8##		-	-	-	-	-	-	-	↓	-	-	-	-	-	-	↓	-	-	-	10	-	-	1,3,4,14		
9		-	-	-	-	-	-	-		-	-	-	-	-	-		-	-	10	-	-	-	1,3,4,8,14		
9**		-	-	-	-	-	-	-		-	-	-	-	-	-		-	-	-	-	-	-	1,3,4,14		
12		-	-	-	-	-	-	-		-	-	-	-	-	-		-	-	3	-	-	-	1,4,5,6,7,10,14		
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	14	-	↓	13	1,3,4,5,6,7,10			
Switching Time	t	1+2-	-	-	-	30	-	-	ns	-	-	-	30	-	-	ns	Pulse In	Pulse Out	-	-	11	-	3,4,14		
		1-2+	-	-	45	-	-	-		45	-	-	-	1	2		-	-	-	-	3,4,14				
		14+13-	-	-	30	-	-	-		30	-	-	-	14	13		-	-	-	-	1,3,4				
		14-13+	-	-	45	-	-	-		45	-	-	-	14	13		-	-	↓	-	-	1,3,4			

MC787P, MC887P (continued)

FIGURE 1 — CLOCK PULSE DEFINITION

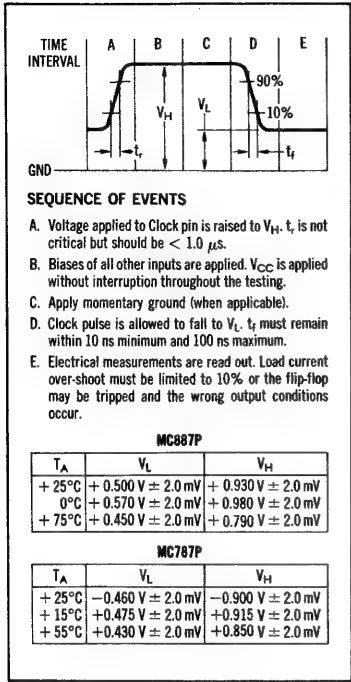


FIGURE 2 — TOGGLE MODE TEST CIRCUIT

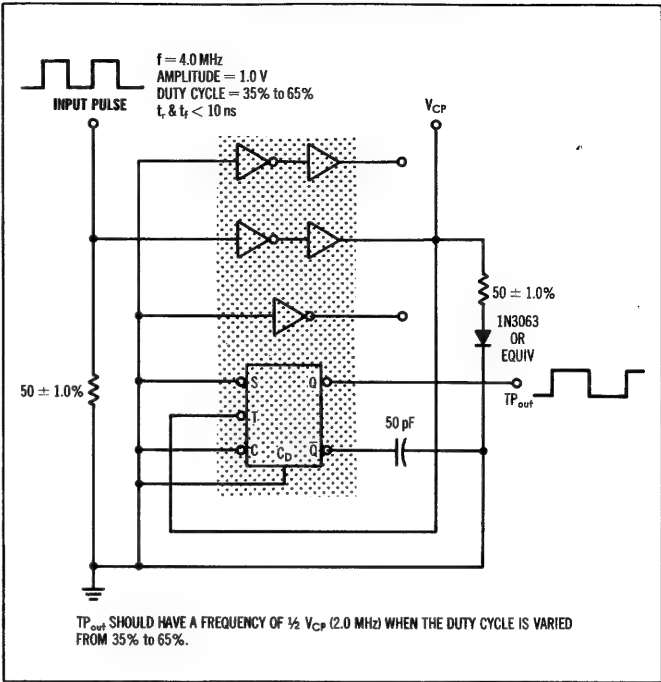
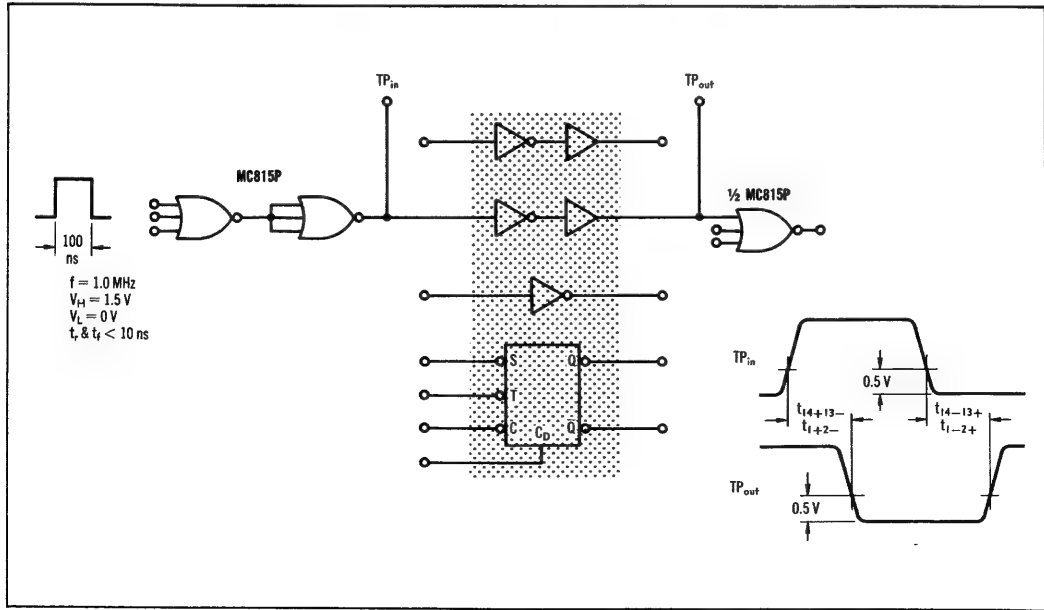
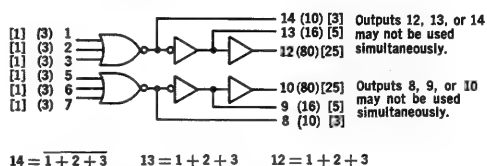


FIGURE 3 — SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



## PLASTIC mW MRTL MC700P/800P series

Two 3-input positive logic NOR gates, each followed by an inverting and non-inverting high fan-out amplifier, are provided in a single package. For each section, the output from each stage is available. If more than one output is used, the full loading factors cannot be employed since each output provides the drive for the succeeding stage.

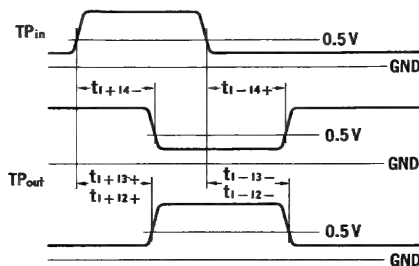


NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL  
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL

$t_{pd} = 24 \text{ ns}$   
 $P_D = 145 \text{ mW (Input Low)}$   
 $56 \text{ mW (Inputs Low)}$

The figure consists of two parts. The top part is a timing diagram showing a square wave pulse with a peak voltage of 1.0 V and a pulse width of 100 ns. The bottom part is a circuit diagram for the MC815P. The input is connected to a 1N3063 diode (or equivalent) in series with a 225 ohm resistor. The output is connected to a 1N3063 diode (or equivalent) in series with a 25 ohm resistor. The output is also connected to a 200 pF capacitor. The circuit includes a shaded area representing the input pins, with a note 'GROUND UNUSED INPUT PINS'. The output is labeled 'TP<sub>out</sub>'.

**Test each output independently. For each test, use only the load associated with the output under test (pin 13 test uses the same load as pin 14 test). Outputs not under test should be left open.**



## ELECTRICAL CHARACTERISTICS

Test procedures are shown for one buffer only.  
The other buffer is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC888P Test Limits							MC788P Test Limits							TEST VOLTAGE APPLIED TO PINS LISTED BELOW:							Gnd
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	V <sub>R</sub> *		
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	V <sub>R</sub> *		
Input Current	I <sub>in</sub>	1 2 3	-	600	-	600	-	570	μA <sub>dc</sub>	-	500	-	500	-	470	μA <sub>dc</sub>	1 2 3	-	2, 3 1, 3 1, 2	-	11	-	4	
Output Current	I <sub>AB</sub>	12	15.0	-	15.0	-	14.25	-	mA <sub>dc</sub>	13.50	-	13.75	-	12.50	-	mA <sub>dc</sub>	-	12	-	14	11	-	4	
	I <sub>A5</sub>	13	3.0	-	3.0	-	2.85	-	↓	2.65	-	2.65	-	2.50	-	mA <sub>dc</sub>	-	13	-	14	↓	-	↓	
	I <sub>A3</sub>	14	1.8	-	1.8	-	1.71	-	↓	-	-	-	-	-	-	-	-	14	-	1, 2, 3	↓	-	↓	
Output Voltage	V <sub>out</sub>	12	-	500	-	400	-	400	mV <sub>dc</sub>	-	400	-	300	-	320	mV <sub>dc</sub>	-	14	-	-	11	12	1,2,3,4	
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	14	-	-	↓	-	1,2,3,4	
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	-	-	↓	-	2,3,4	
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2	-	-	↓	-	1,3,4	
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	-	1,2,4	
Saturation Voltage	V <sub>CE(sat)</sub>	12	-	400	-	300	-	350	mV <sub>dc</sub>	-	300	-	290	-	320	mV <sub>dc</sub>	-	-	14	-	11	12	1,2,3,4	
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	14	-	-	↓	-	1,2,3,4	
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	-	-	↓	-	2,3,4	
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2	-	-	↓	-	1,3,4	
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	-	1,2,4	
Switching Time	t	1+12+	-	-	-	65	-	-	-	-	-	-	65	-	-	-	Pulse In	Pulse Out	-	-	11	-	2,3,4	
		1-12-	-	-	-	58	-	-	-	-	-	-	58	-	-	-	1	12	-	-	↓	-	↓	
		1+13+	-	-	-	42.5	-	-	-	-	-	-	42.5	-	-	-	1	13	-	-	↓	-	↓	
		1-13-	-	-	-	42.5	-	-	-	-	-	-	42.5	-	-	-	1	13	-	-	↓	-	↓	
		1+14+	-	-	-	20	-	-	-	-	-	-	20	-	-	-	1	14	-	-	↓	-	↓	
		1-14-	-	-	-	28	-	-	-	-	-	-	28	-	-	-	1	14	-	-	↓	-	↓	

Ground input pins of buffer not under test. Other pins not listed are left open. \*Resistor value to V<sub>CC</sub>

TEST VOLTAGE VALUES						
(Volts)						(Ohms)
V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	V <sub>R</sub> *	
0.960	0.930	1.80	0.570	3.60	640	
0.910	0.880	1.80	0.500	3.60	640	
0.820	0.790	1.80	0.450	3.60	750	
0.865	0.865	1.80	0.475	3.60	640	
0.850	0.850	1.80	0.460	3.60	640	
0.800	0.800	1.80	0.430	3.60	640	

@ Test Temperature

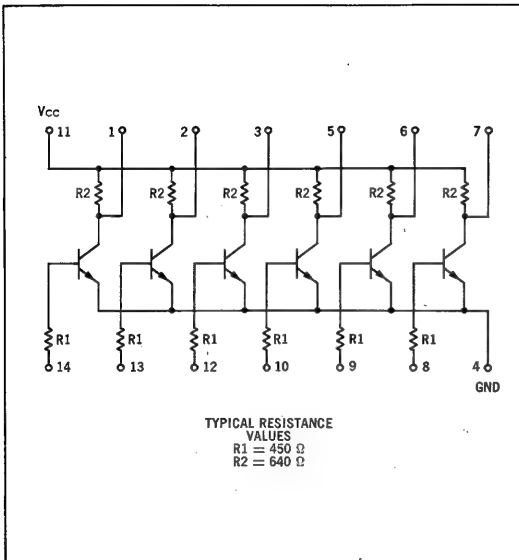
MC888P { 0°C  
+25°C  
+75°C

MC788P { +15°C  
+25°C  
+55°C

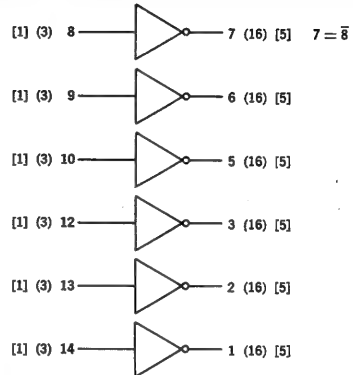
# HEX INVERTERS

# PLASTIC MRTL MC700P/800P series

## MC789P • MC889P



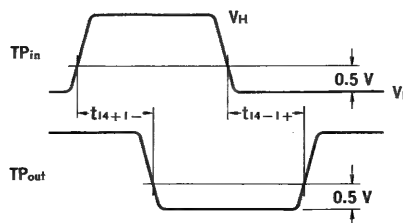
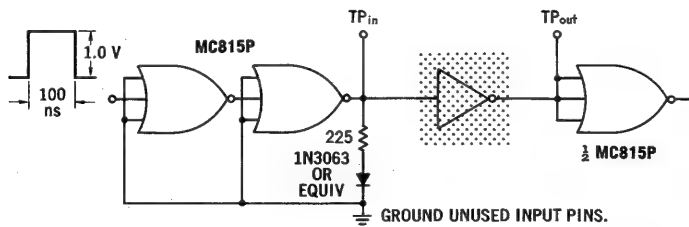
Six individual circuits are contained in a single package. Each provides the simple inversion function.



NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL  
 NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL

$t_{pd} = 12$  ns  
 $P_D = 130$  mW (Input High)  
 15 mW (Inputs Low)

## SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one inverter only.  
The other inverters are tested in the same manner.

@ Test Temperature		TEST VOLTAGE VALUES						
		(Volts)						
		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>		
MC889P	{	0°C	0.960	0.930	1.80	0.570	3.60	
		+25°C	0.910	0.880	1.80	0.500	3.60	
		+75°C	0.820	0.790	1.80	0.450	3.60	
MC789P	{	+15°C	0.865	0.865	1.80	0.475	3.60	
		+25°C	0.850	0.850	1.80	0.460	3.60	
		+55°C	0.800	0.800	1.80	0.430	3.60	

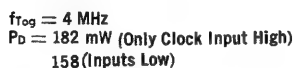
t Limits			TEST VOLTAGE					Gnd
+55°C		Unit	APPLIED TO PINS LISTED BELOW:					
Min	Max		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	
-	470	μA <sub>dc</sub>	14	-	*	-	11	4
2.5	-	mA <sub>dc</sub>	1	-	-	14	11	4
-	320	mV <sub>dc</sub>	-	14	-	-	11	4
-	320	mV <sub>dc</sub>	-	-	14	-	11	4
-	-	ns	Pulse In	Pulse Out				
-	-	ns	14	1	-	-	11	4

Ground inputs of inverters not under test. Other pins not listed are left open

\* To simulate worse case conditions, the output of inverter under test is tied to the output of another inverter which has its input taken to V<sub>BOT</sub>

## PLASTIC MRTL MC700P/800P series

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.

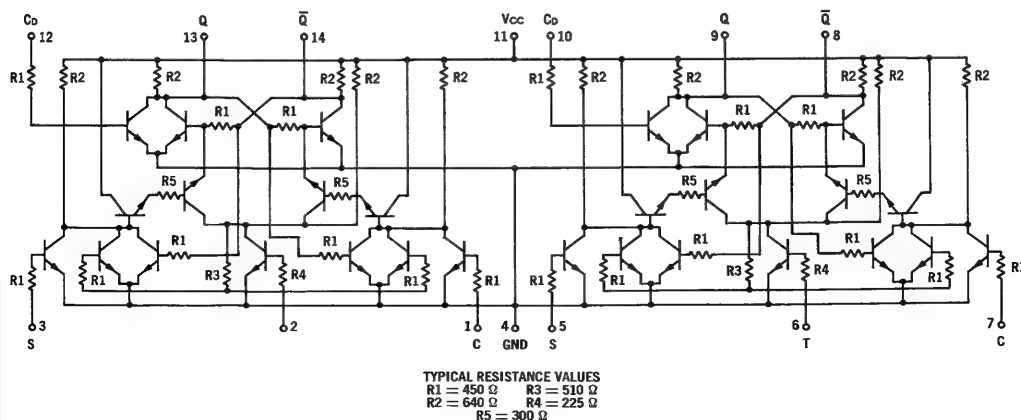


### CLOCKED INPUT OPERATION ①

$t_n$ ②		$t_{n+1}$ ②	
S	C	Q	$\bar{Q}$
1	1	$Q_n$ ③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	$Q_n$ ③

1. Direct input ( $C_0$ ) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted  $t_n$  and the time period subsequent to this transition is denoted  $t_{n+1}$ .
3.  $Q_n$  is the state of the Q output in the time period  $t_n$ .
4. Clock pulse fall time must be  $< 100$  ns.

NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL  
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL



# ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.  
The other flip-flop is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC890P Test Limits							MC790P Test Limits							TEST VOLTAGE						Gnd
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	APPLIED TO PINS LISTED BELOW:						
																	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	
Input Current	I <sub>in</sub>	1	-	600	-	600	-	570	μA <sub>dc</sub>	-	500	-	500	-	470	μA <sub>dc</sub>	1	-	13	-	11	2, 3, 4, 12	
	2I <sub>in</sub>	2	-	1200	-	1200	-	1140	↓	-	1000	-	1000	-	940	↓	2	-	1, 3	-	↓	4, 12	
	I <sub>in</sub>	3	-	600	-	600	-	570	↓	-	500	-	500	-	470	↓	3	-	14	-	↓	1, 2, 4, 12	
	I <sub>in</sub>	12	-	600	-	600	-	570	↓	-	500	-	500	-	470	↓	12	-	14	-	↓	1, 2, 3, 4	
Output Current	I <sub>A3</sub>	13	1.80	-	1.80	-	1.71	-	mA <sub>dc</sub>	1.65	-	1.65	-	1.56	-	mA <sub>dc</sub>	-	13	1	12	11	2, 3, 4	
		14	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	14	3, 12	-	↓	1, 2, 4		
		14	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	-	12, 14	3	-	↓	1, 2, 4	
Output Voltage	V <sub>out</sub>	13	-	500	-	400	-	400	mV <sub>dc</sub>	-	400	-	300	-	320	mV <sub>dc</sub>	-	12	-	-	11	1, 2, 3, 4, 14	
		13*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1, 3	-	-	↓	4, 12	
		13*##	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	-	3	↓	↓	
		13*###	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1, 3	↓	↓	
		14*##	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1, 3	-	-	↓	↓	
		14*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	1	↓	↓	
		14*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1, 3	↓	↓	
Saturation Voltage	V <sub>CE(sat)</sub>	13	-	400	-	300	-	350	mV <sub>dc</sub>	-	300	-	290	-	320	mV <sub>dc</sub>	-	-	12	-	11	1, 2, 3, 4, 14	
		13#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	↓	1, 2, 3, 4, 12	
		14##	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	12	-	↓	1, 2, 3, 4	

Ground unused input pins. Other pins not listed are left open.

\* Clock pulse to pin 2, see Figure 1,

# Pin 13 = LOW } Set by a momentary ground prior to the  
## Pin 14 = LOW } application of the negative-going Clock Pulse.

@ Test

Temperature

0°C

+25°C

+75°C

+15°C

+25°C

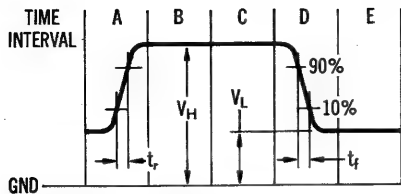
+55°C

## TEST VOLTAGE VALUES

(Volts)

V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>
0.960	0.930	1.80	0.570	3.60
0.910	0.880	1.80	0.500	3.60
0.820	0.790	1.80	0.450	3.60
0.865	0.865	1.80	0.475	3.60
0.850	0.850	1.80	0.460	3.60
0.800	0.800	1.80	0.430	3.60

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

- A. Voltage applied to Clock pin is raised to  $V_H$ .  $t_r$  is not critical but should be  $< 1.0 \mu s$ .
- B. Biases of all other inputs are applied.  $V_{CC}$  is applied without interruption throughout the testing.
- C. Apply momentary ground (when applicable).
- D. Clock pulse is allowed to fall to  $V_L$ .  $t_f$  must remain within 10 ns minimum and 100 ns maximum.
- E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

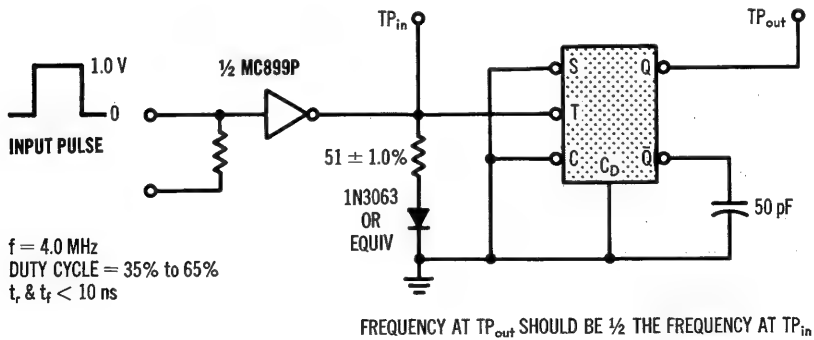
MC890P

$T_A$	$V_L$	$V_H$
+ 25°C	+0.500 V $\pm$ 2.0 mV	+0.930 V $\pm$ 2.0 mV
0°C	+0.570 V $\pm$ 2.0 mV	+0.980 V $\pm$ 2.0 mV
+ 75°C	+0.450 V $\pm$ 2.0 mV	+0.840 V $\pm$ 2.0 mV

MC790P

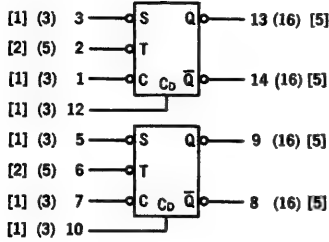
$T_A$	$V_L$	$V_H$
+ 25°C	+ 0.460 V $\pm$ 2.0 mV	+0.900 V $\pm$ 2.0 mV
+ 15°C	+ 0.475 V $\pm$ 2.0 mV	+0.915 V $\pm$ 2.0 mV
+ 55°C	+ 0.430 V $\pm$ 2.0 mV	+0.850 V $\pm$ 2.0 mV

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



**MC791P • MC891P**

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



$f_{reg} = 4 \text{ MHz}$   
 $t_{pd} = 40 \text{ ns typ}$

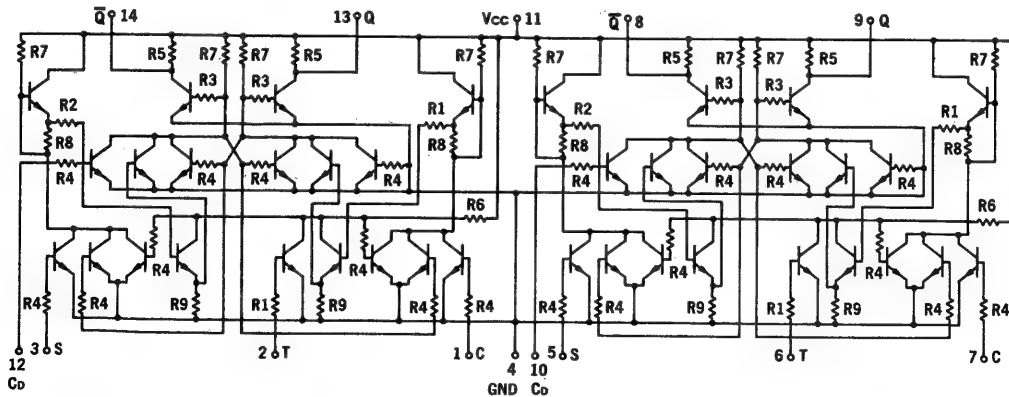
$P_o = 190 \text{ mW typ (Only Clock Input High)}$   
 $160 \text{ mW typ (Inputs Low)}$

**CLOCKED INPUT OPERATION ①**

$t_n$ ②		$t_{n+1}$ ③	
S	C	Q	$\bar{Q}$
1	1	$Q_n$ ④	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	$Q_n$ ④

1. Direct input ( $C_o$ ) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted  $t_n$  and the time period subsequent to this transition is denoted  $t_{n+1}$ .
3.  $Q_n$  is the state of the Q output in the time period  $t_n$ .

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR mW MRTL  
 NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL



**TYPICAL RESISTANCE VALUES**  
 $R1 = 300 \Omega$   $R4 = 600 \Omega$   $R7 = 900 \Omega$   
 $R2 = 500 \Omega$   $R5 = 640 \Omega$   $R8 = 2.0 k$   
 $R3 = 550 \Omega$   $R6 = 700 \Omega$   $R9 = 3.0 k$

## ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.  
The other flip-flop is tested in the same manner.

																TEST VOLTAGE VALUES									
																(Volts)									
																V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>					
<div><div>MC891P</div><div>MC791P</div></div>																0°C					0.960	0.930	1.80	0.570	3.60
																+25°C					0.910	0.880	1.80	0.500	3.60
																+75°C					0.820	0.790	1.80	0.450	3.60
																+15°C					0.865	0.865	1.80	0.475	3.60
																+25°C					0.850	0.850	1.80	0.460	3.60
																+55°C					0.800	0.800	1.80	0.430	3.60
Characteristic	Symbol	Pin Under Test	MC891P Test Limits								MC791P Test Limits								TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					Gnd	
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>				
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max										
Input Current	I <sub>in</sub>	1 †	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	-	-	11	4			
	2I <sub>in</sub>	2	-	1200	-	1200	-	1140	μAdc	-	1000	-	1000	-	940	μAdc	2	-	1, 3	-	11	4			
	I <sub>in</sub>	3	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	3	-	12	-	11	4			
	I <sub>in</sub>	12	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	12	-	-	-	11	4			
Output Current	I <sub>A5</sub>	13 †	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	13	-	-	11	-			
		14	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	12, 14	-	-	11	4			
Output Voltage	V <sub>out</sub>	13 § ⑤	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	4, 12			
		13 §§ ④	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	3	↓	↓			
		13 § ⑥	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	-	-	↓	↓			
		13 §§ ⑦	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	3	↓	↓			
		14 § ④	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1	↓	↓			
		14 §§ ⑤	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	↓			
		14 § ⑦	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1	↓	↓			
		14 §§ ⑥	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	↓			
Saturation Voltage	V <sub>CE(sat)</sub>	13 †	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	12	-	-	11	4			
		13*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1, 3	-	-	↓	↓			
		13 †*	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	-	-	↓	↓			
		13 †*	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	3	↓	↓			
		14*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	1, 3	↓			
		14*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1	↓	↓			
		14 †*	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1, 3	-	-	↓	↓			

Ground inputs of flip-flop not under test. Other pins not listed are left open.

† Preset the flip-flop by the following procedure:

- (1) Momentarily apply V<sub>BOT</sub> to pin 12 to preclear flip-flop.
- (2) After V<sub>BOT</sub> is removed from pin 12, ground pins 1 and 3.
- (3) Apply a negative-going clock pulse to pin 2 (see note\*) while pins 1 and 3 are still grounded. This changes the state of the flip-flop to the SET condition.
- (4) Remove grounds from pins 1 and 3, and proceed with the test.

\* Clock pulse to pin 2, see Figure 1.

# Pin 12 = HIGH — Set by momentary application of V<sub>BOT</sub> prior to the application of the negative-going clock pulse.

§ = Clock pulse to pin 2, data pulse to pin 3.  
§§ = Clock pulse to pin 2, data pulse to pin 1.

- ④ = See Figure 4.  
⑤ = See Figure 5.  
⑥ = See Figure 6.  
⑦ = See Figure 7.

MC791P, MC891P (continued)

FIGURE 1 — CLOCK PULSE DEFINITION

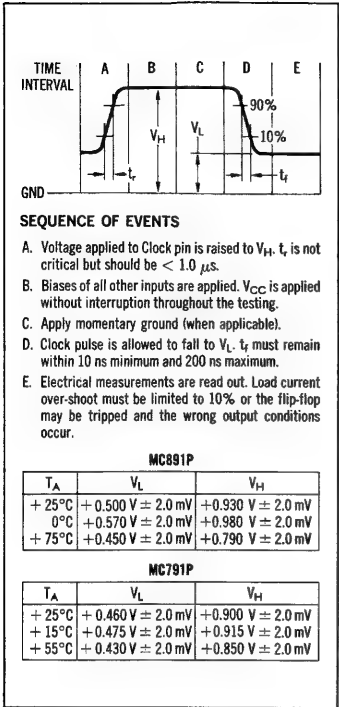


FIGURE 2 — TOGGLE MODE TEST CIRCUIT

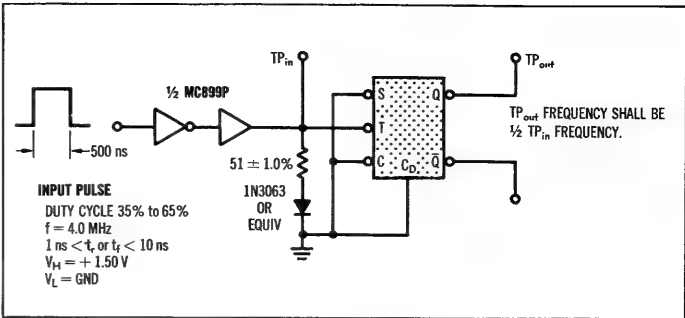


FIGURE 3 — TEST CIRCUIT

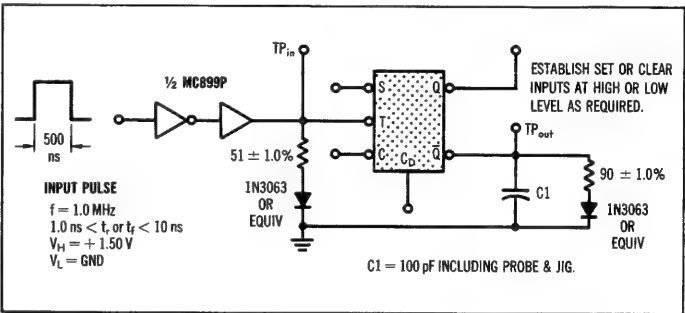


FIGURE 4 — TEST WAVEFORMS

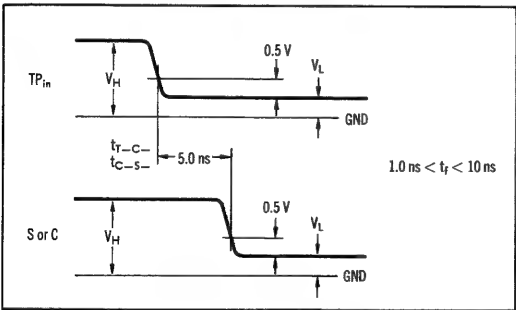


FIGURE 5 — TEST WAVEFORMS

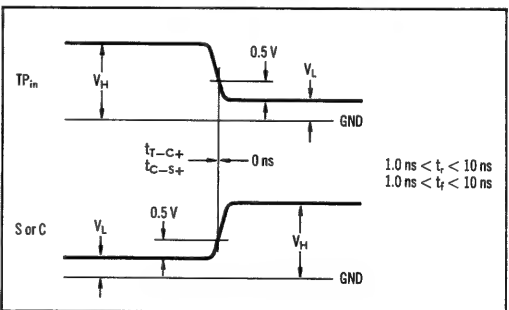


FIGURE 6 — TEST WAVEFORMS

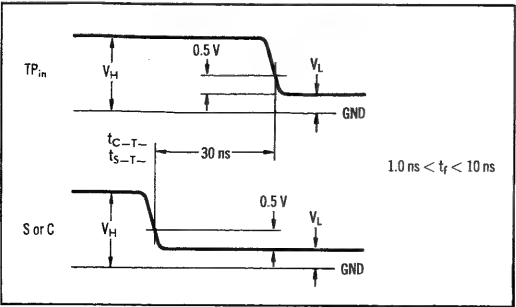
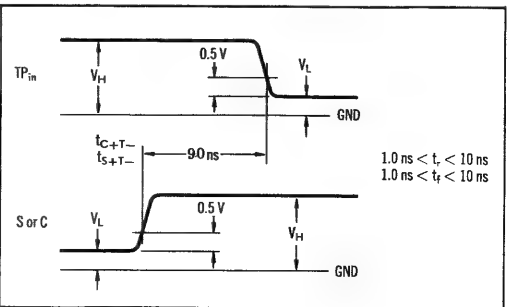
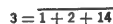
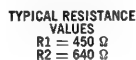


FIGURE 7 — TEST WAVEFORMS



## PLASTIC MRTL MC700P/800P series

Three 3-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.

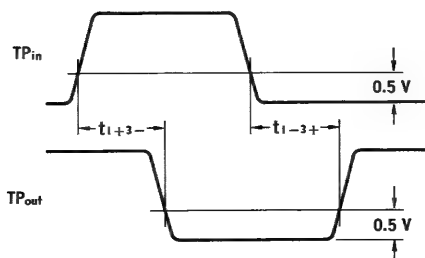


NUMBER IN PARENTHESES INDICATES  
LOADING FACTOR FOR mW MRTL

NUMBER IN BRACKETS INDICATES  
LOADING FACTOR FOR MRTL

$t_{pd} = 12 \text{ ns}$   
 $P_D = 82 \text{ mW (Input High)}$   
 $24 \text{ mW (Inputs Low)}$

The timing diagram shows a square wave input signal with a period of 100 ns and a frequency of 1.0 MHz. The input signal is connected to the MC815P. The output signal, labeled TP<sub>in</sub>, is shown with a delay and a rise time of less than 10 ns. The output signal is then connected to the 1/2 MC815P, which produces the final output signal, labeled TP<sub>out</sub>. The output signal is shown with a delay and a rise time of less than 10 ns. The diagram also shows the input signal connected to the 1/2 MC815P, which produces the final output signal, labeled TP<sub>out</sub>. The output signal is shown with a delay and a rise time of less than 10 ns.





## ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.  
The other gates are tested in the same manner.

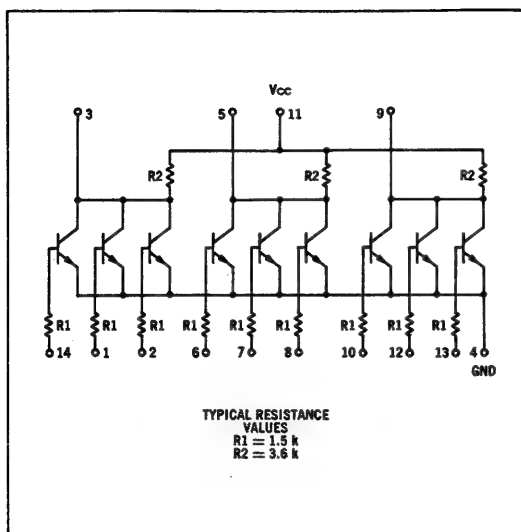
Characteristic	Symbol	Pin Under Test	MC892P Test Limits							MC792P Test Limits							TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					Gnd
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	V <sub>in</sub>	V <sub>on</sub>	V <sub>Bot</sub>	V <sub>off</sub>	V <sub>cc</sub>	
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max							
			1	2	14	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	
Input Current	I <sub>in</sub>	1 2 14	-	600	-	600	-	570	μA <sub>dc</sub>	-	500	-	500	-	470	μA <sub>dc</sub>	1 2 14	-	2, 14 1, 14 1, 2	-	11	4
Output Current	I <sub>A5</sub>	3	3.00	-	3.00	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	3	-	1, 2, 14	11	4
Output Voltage	V <sub>out</sub>	3 3 3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	14 1 2	-	-	11	1,2,4 2,4,14 1,4,14
Saturation Voltage	V <sub>CE(sat)</sub>	3 3 3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	14 1 2	-	11	1,2,4 2,4,14 1,4,14
Switching Time	t <sub>on</sub> + t <sub>off</sub>	1, 3	-	-	-	48	-	-	ns	-	-	-	48	-	-	ns	Pulse In	Pulse Out	-	-	11	2,4,14

Ground input pins of gates not under test. Other pins not listed are left open.

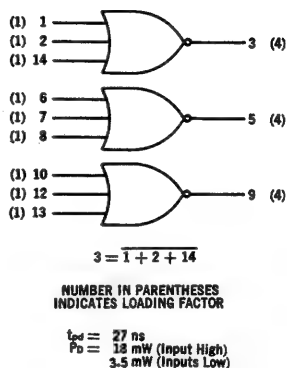
@ Test Temperature		TEST VOLTAGE VALUES				
		(Volts)				
		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>
MC892P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC792P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

## PLASTIC mW MRTL MC700P/800P series

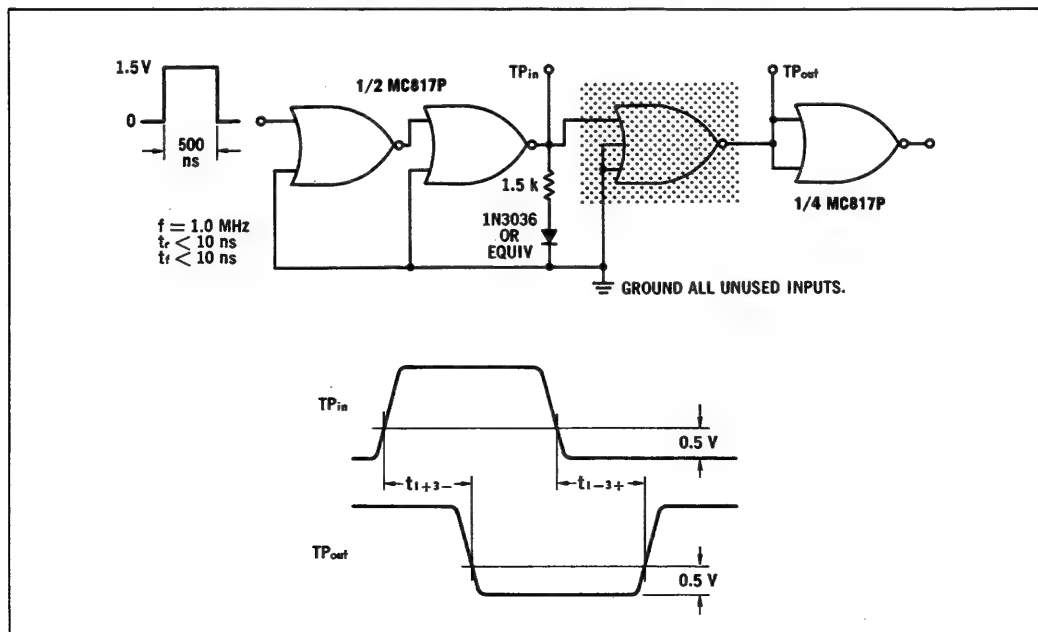
## MC793P • MC893P



Three 3-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.



### SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



# ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.  
The other gates are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES				
		(Volts)				
		V <sub>in</sub>	V <sub>on</sub>	V <sub>bot</sub>	V <sub>off</sub>	V <sub>cc</sub>
MC893P	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60
MC793P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC893P Test Limits							MC793P Test Limits							TEST VOLTAGE APPLIED TO PINS LISTED BELOW:						Gnd	
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>			
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max									
Input Current	I <sub>in</sub>	1 2 14	-	150	-	140	-	140	μA <sub>dc</sub> ↓	-	150	-	150	-	150	μA <sub>dc</sub> ↓	1 2 14	-	2, 14 1, 14 1, 2	-	11	↓	4	↓
Output Current	I <sub>A4</sub>	3	570	-	570	-	535	-	μA <sub>dc</sub>	570	-	570	-	570	-	μA <sub>dc</sub>	-	3	-	1,2,14	11	4		
Output Voltage	V <sub>out</sub>	3 3 3	-	400	-	350	-	300	mV <sub>dc</sub> ↓	-	400	-	300	-	320	mV <sub>dc</sub> ↓	-	14 1 2	-	-	11	1,2,4 2,4,14 1,4,14		
Saturation Voltage	V <sub>CE(sat)</sub>	3 3 3	-	250	-	250	-	250	mV <sub>dc</sub> ↓	-	220	-	230	-	320	mV <sub>dc</sub> ↓	-	-	14 1 2	-	11	1,2,4 2,4,14 1,4,14		
Switching Time	t <sub>on</sub> + t <sub>off</sub>	1, 3	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	Pulse In 1	Pulse Out 3	-	-	11	2,4,14		

Ground input pins of gates not under test. Other pins not listed are left open.

# SERIAL-PARALLEL SHIFT REGISTER

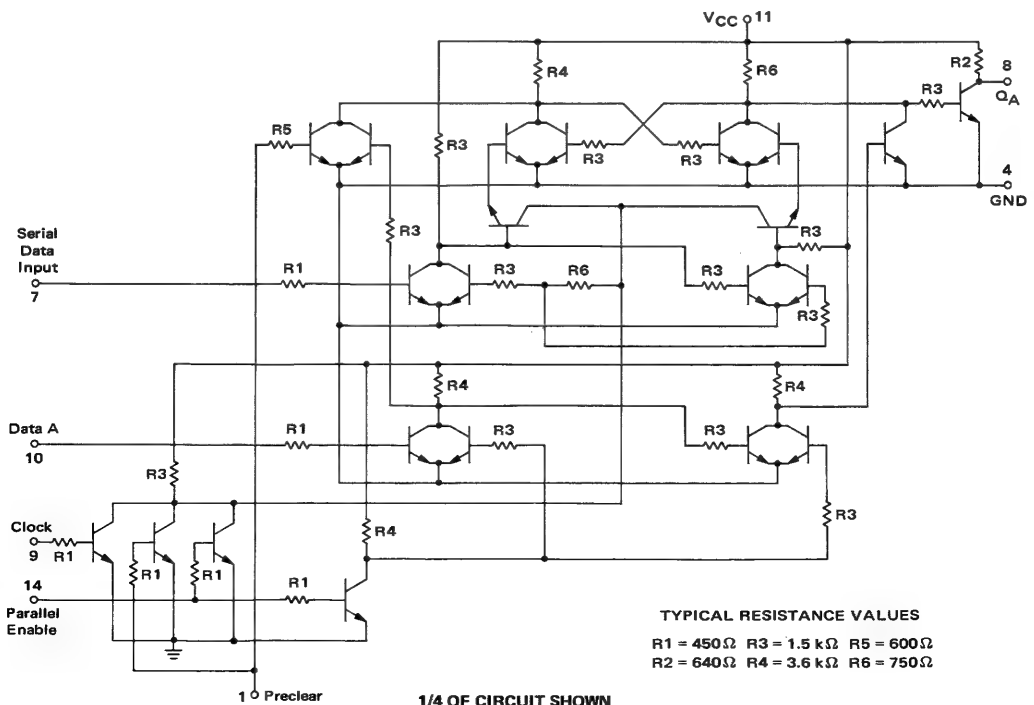
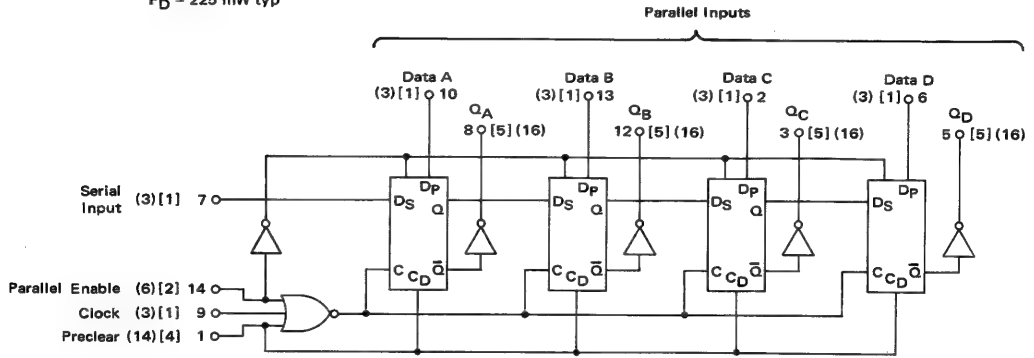
# PLASTIC MRTL MC700P/800P series

## MC794P • MC894P\*

Number in parenthesis indicates mW MRTL loading factor. Number in brackets indicates MRTL loading factor.

$t_{pd} = 55 \text{ ns typ}$   
 $P_D = 225 \text{ mW typ}$

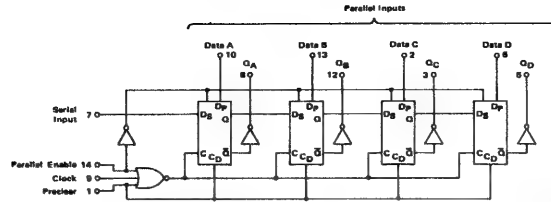
The MC794P/MC894P is a highly versatile 4-bit Shift Register with both Serial and Parallel entry capability. It can be utilized as an accumulator, buffer register, serial to parallel/parallel to serial converter, and is fully compatible with the other MRTL functions. The clock fall time must be  $\leq 100 \text{ ns}$ .



\*See General Information section for packaging.

# ELECTRICAL CHARACTERISTICS

Test procedures for Inputs B, C, and D are the same as given for Input A (pin 10) in the table below.



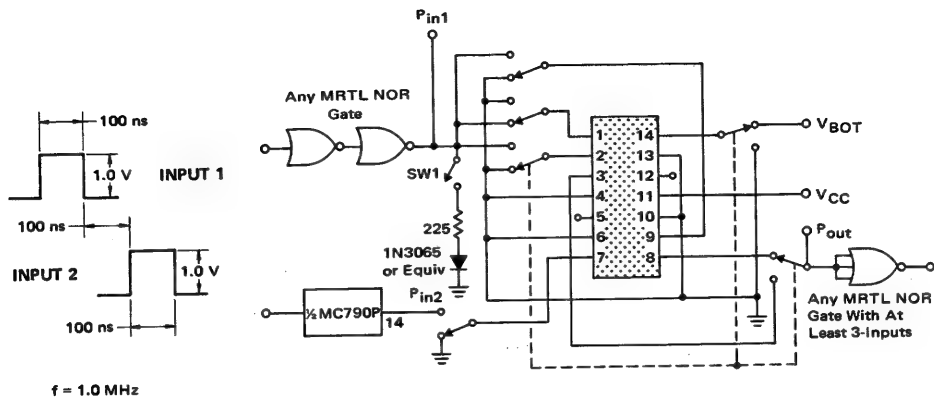
TEST VOLTAGE VALUES									
(Volts)									
@ Test Temperature									
MC894P									
MC794P									
TEST VOLTAGE APPLIED TO PINS LISTED BELOW:									
Gnd									
V <sub>in</sub> V <sub>on</sub> V <sub>BOT</sub> V <sub>off</sub> V <sub>CC</sub>									
0°C									
+25°C									
+75°C									
+15°C									
+25°C									
+55°C									
Pin Under Test									
Characteristic									
Symbol									
MC894P Test Limits									
MC794P Test Limits									
Unit									
Min Max Min Max Min Max Min Max Min Max Min Max Min Max Min Max									
Input Current									
Output Current									
Output Voltage									
Power Supply Drain Current									
Switching Times									
t <sub>2-3-</sub> t <sub>2+3+</sub> t <sub>1+8-</sub> t <sub>1-8+</sub> t <sub>9-8-</sub> t <sub>9-8+</sub>									
ns									
P <sub>in1</sub> P <sub>in2</sub> P <sub>out</sub>									
14 11									
1,4,6,7,9,10,13									
1,4,6,7,9,10,13,14									
2,4,6,7,9,10,13,14									
1,2,4,6,10,13,14									
1,2,4,6,10,13,14									

Ground all unused input pins. Other pins not listed are left open.

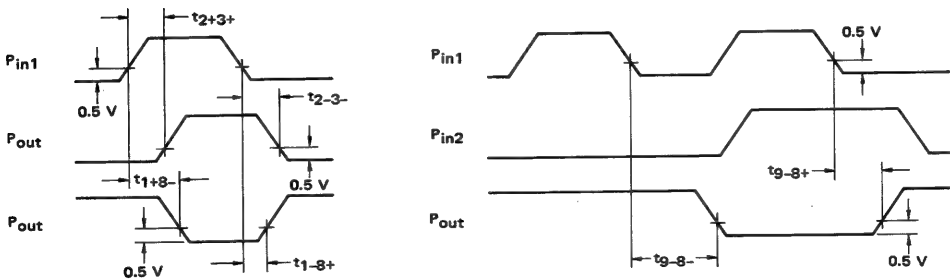
\*See "Switching Times Test Circuit and Waveforms".

# MC794P, MC894P (continued)

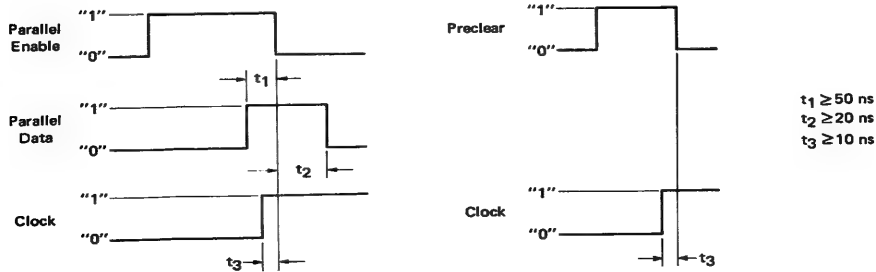
## SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



SW1 is open only when testing pin 1, remains closed for all other tests.



## PARALLEL ENABLE MODE



# DUAL FULL ADDERS

# PLASTIC MRTL MC700P/800P series

## MC796P • MC896P

TRUTH TABLE

INPUT LOGIC LEVEL			OUTPUT LOGIC LEVEL	
A	B	C <sub>i</sub>	S	C <sub>o</sub>
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Provides the SUM and CARRY functions while requiring only the AUGEND (A) and ADDEND (B) inputs with CARRY IN.

### POSITIVE LOGIC

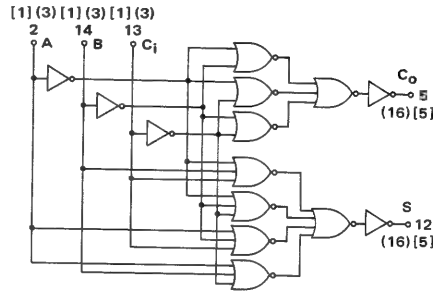
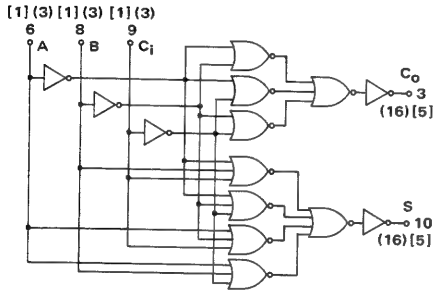
$$C_o = ABC_i + AB\bar{C}_i + A\bar{B}C_i + \bar{A}BC_i$$

$$S = ABC_i + AB\bar{C}_i + \bar{A}BC_i + \bar{A}\bar{B}\bar{C}_i$$

$$t_{pd} = 60 \text{ ns typ}$$

$$P_D = 225 \text{ mW typ}$$

Number in Parenthesis Indicates mWMRTL Loading Factor.  
Number in Brackets Indicates MRTL Loading Factor.



## ELECTRICAL CHARACTERISTICS

Test procedures are shown for one full adder only. The other full adder is tested in the same manner.

@Test Temperature	TEST VOLTAGE VALUES (Volts)					
	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	
	0°C	+25°C	+75°C	+15°C	+25°C	+55°C
MC896P	0.960	0.930	1.80	0.570	3.60	
	0.910	0.800	1.80	0.500	3.60	
	0.820	0.790	1.80	0.450	3.60	
MC796P	0.885	0.865	1.80	0.475	3.60	
	0.850	0.850	1.80	0.460	3.60	
	0.800	0.800	1.80	0.430	3.60	

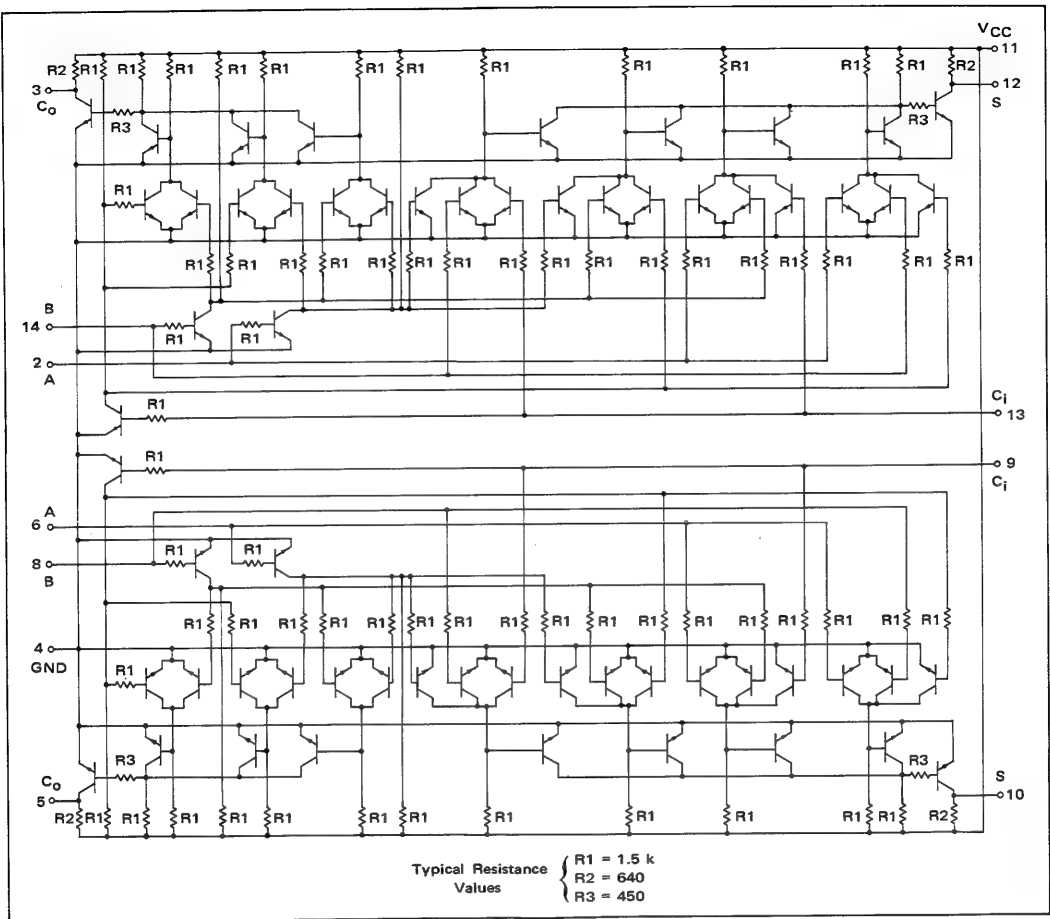
  

TEST VOLTAGE APPLIED TO PINS LISTED BELOW:										
V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	Gnd					
2	13	14	11	4						
13	14	11	4							
14	11	4								
11	4									
4										

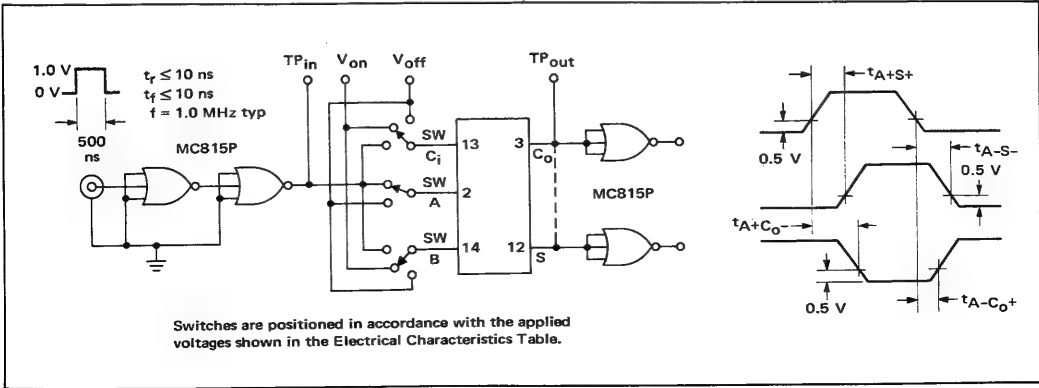
		Pin		MC896P Test Limits						MC796P Test Limits						TEST VOLTAGE		0.800		0.800		1.80		0.430		3.60		
Characteristic	Symbol	Under Test	0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	APPLIED TO PINS LISTED BELOW:						V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	Gnd
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		Min	Max	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>						
Input Current	I <sub>in</sub>	2 13 14	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	2 13 14	-	-	-	-	-	-	-	11	4	4	
Output Current	I <sub>AS</sub>	3  12	3.00	-	3.00	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	3,13,14 2,3,13 2,3,14 (2,3,) (13,14)	-	-	2 14 13	-	-	11	4	4		
Output Voltage	V <sub>out</sub>	3  12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	-	-	2,13,14 2,14 2	-	-	11	4	4			
Switching Time																												
	t <sub>2-12</sub>	12	-	-	-	75	-	ns	-	-	-	75	-	-	ns		Pulse In		Pulse Out									
	t <sub>2-13</sub>	12	-	-	-	75	-	-	-	-	-	75	-	-	-	2	13,14		12	-	-	11	4	4				
	t <sub>2-3</sub>	3	-	-	-	65	-	-	-	-	-	85	-	-	-		13		3	14								
	t <sub>2-3</sub>	3	-	-	-	65	-	-	-	-	-	65	-	-	-		13		3	14								
	t <sub>14-12</sub>	12	-	-	-	75	-	-	-	-	-	75	-	-	-	14	-	12	2,13									
	t <sub>14-12</sub>	12	-	-	-	75	-	-	-	-	-	75	-	-	-		-	12	2,13									
	t <sub>14-3</sub>	3	-	-	-	85	-	-	-	-	-	85	-	-	-		13		3	2								
	t <sub>14-3</sub>	3	-	-	-	65	-	-	-	-	-	65	-	-	-		13		3									
	t <sub>13-12</sub>	13	-	-	-	70	-	-	-	-	-	70	-	-	-	13	14	12	3									
	t <sub>13-12</sub>	13	-	-	-	80	-	-	-	-	-	80	-	-	-		12		3									
	t <sub>13-3</sub>	3	-	-	-	70	-	-	-	-	-	70	-	-	-		3		3									
	t <sub>13-3</sub>	3	-	-	-	80	-	-	-	-	-	80	-	-	-		3		3									

Ground inputs of full adder not under test. Other pins not listed are left open.

# MC796P, MC896P (continued)



## SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





# DUAL FULL SUBTRACTORS

# PLASTIC MRTL MC700P/800P series

## MC797P • MC897P

TRUTH TABLE

INPUT LOGIC LEVEL			OUTPUT LOGIC LEVEL	
X	Y	B <sub>i</sub>	D	B <sub>o</sub>
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Provides the DIFFERENCE and BORROW functions while requiring only MINUEND (X) and SUBTRAHEND BORROW IN.

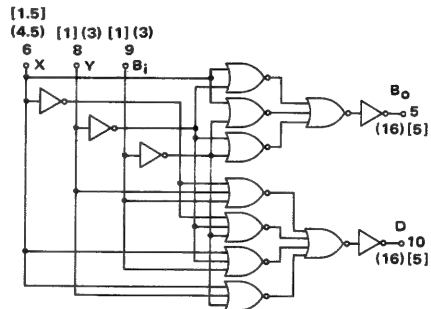
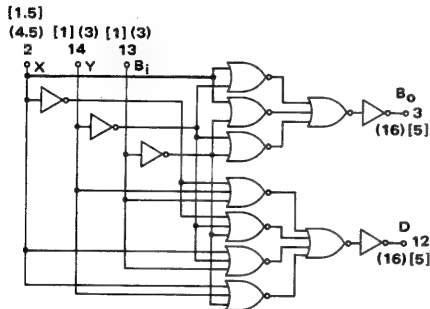
### POSITIVE LOGIC

$$D = Y \times B_i + \bar{Y} \times \bar{B}_i + \bar{Y} \times B_i + Y \times \bar{B}_i$$

$$B_o = \bar{Y} \times B_i + Y \times \bar{B}_i + Y \times B_i + Y \times B_i$$

t<sub>pd</sub> = 60 ns typ  
P<sub>D</sub> = 225 mW typ

Number in Parenthesis Indicates mW MRTL Loading Factor.  
Number in Brackets Indicates MRTL Loading Factor.



### ELECTRICAL CHARACTERISTICS

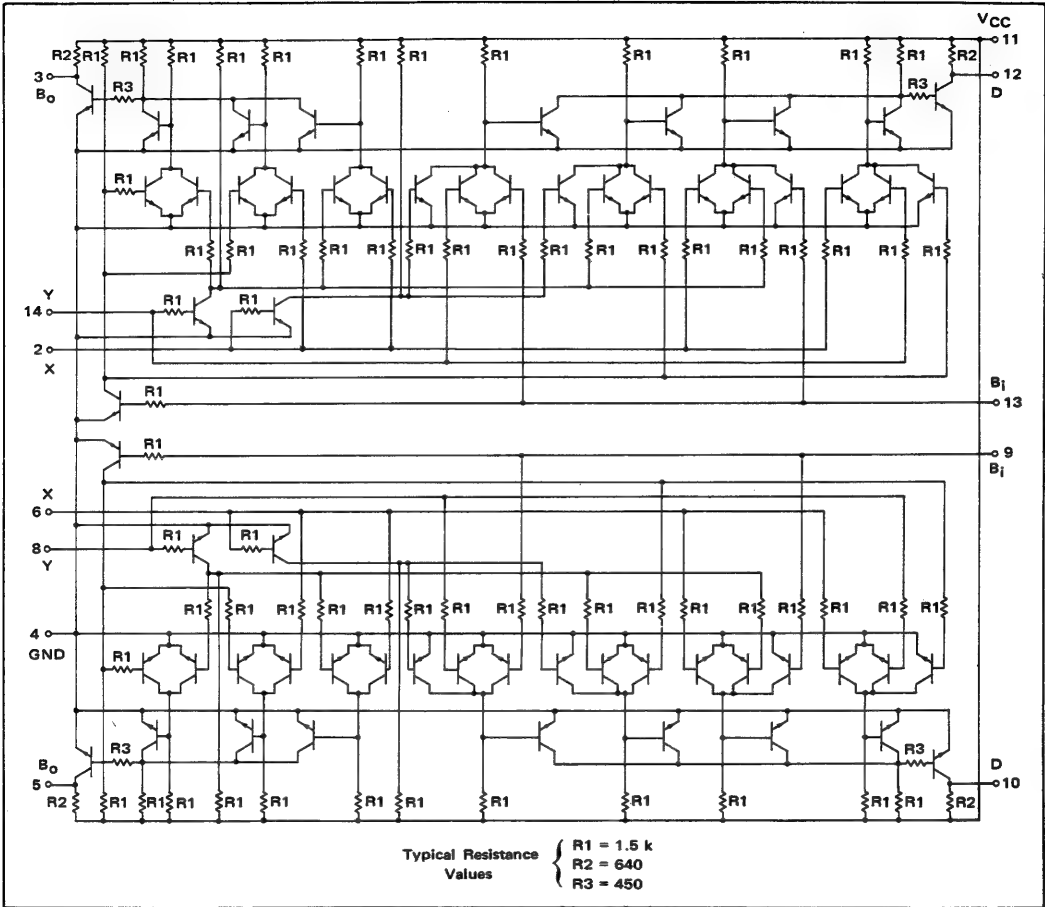
Test procedures are given for only one subtractor. The other subtractor is tested in the same manner.

@Test Temperature	TEST VOLTAGE VALUES (Volts)				
	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>
MC897P	0°C	0.980	0.930	1.80	0.570
	+25°C	0.910	0.800	1.80	0.500
	+75°C	0.830	0.790	1.80	0.450
MC797P	+15°C	0.985	0.885	1.80	0.475
	+25°C	0.950	0.850	1.80	0.480
	+55°C	0.800	0.800	1.80	0.430

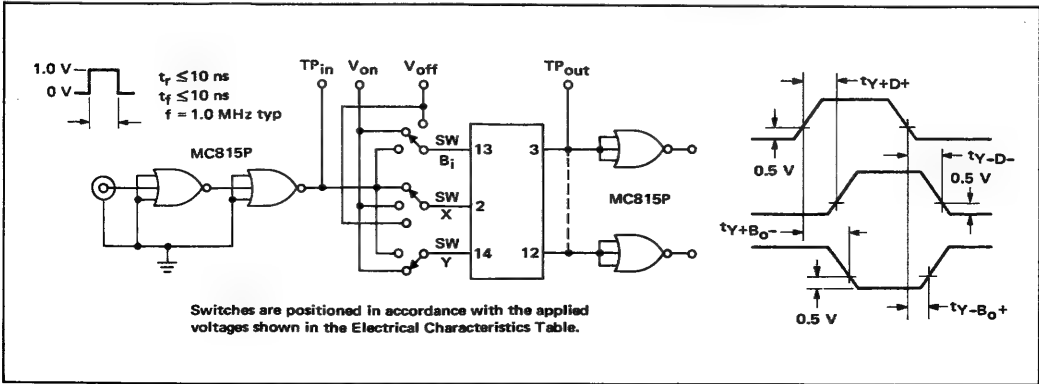
Characteristic	Symbol	Pin Under Test	MC897P Test Limits								MC797P Test Limits								TEST VOLTAGE APPLIED TO PINS LISTED BELOW:						Gnd
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	APPLIED TO PINS LISTED BELOW:								
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>				
Input Current	1.5 I <sub>in</sub> I <sub>in</sub> I <sub>in</sub>	2 3 14	- - -	900 600 600	- - -	900 600 600	- - -	965 570 570	μAdc ↓ ↓	- - -	750 900 500	- - -	750 500 500	- - -	705 470 470	μAdc ↓ ↓	3 13 14	- - -	- - -	- - -	- - -	11 ↓ ↓	4 ↓ ↓		
Output Current	I <sub>AS</sub> ↓ ↓ ↓	3 ↓ ↓ ↓	3.00 - - -	- - -	3.00 - - -	- - -	2.85 - -	- - -	mAdc ↓ ↓ ↓	2.65 - -	- - -	- - -	2.65 - -	- - -	2.50 ↓ ↓ ↓	- - -	mAdc ↓ ↓ ↓	- - -	(2,3, 13,14) 3,13 3,14 12,13 12,14 3,12 (2,12, 13,14)	- - -	- - -	2,14 2,13 2,14 2,15 13,14 -	11 ↓ ↓ ↓ ↓ ↓ ↓	4 ↓ ↓ ↓ ↓ ↓ ↓	
Output Voltage	V <sub>out</sub> ↓ ↓ ↓	3 ↓ ↓ ↓	- - -	500 ↓ ↓ ↓	- - -	400 ↓ ↓ ↓	- - -	400 ↓ ↓ ↓	mVdc ↓ ↓ ↓	- - -	400 ↓ ↓ ↓	- - -	300 ↓ ↓ ↓	- - -	320 ↓ ↓ ↓	- - -	mVdc ↓ ↓ ↓	- - -	2,13 2,14 - - 13,14 2,13 2,13	- - -	14 13 2,13,14 2,13,14 13 14	11 ↓ ↓ ↓ ↓ ↓ ↓	4 ↓ ↓ ↓ ↓ ↓ ↓		
Switching Time	t <sub>2-12+</sub> t <sub>2-12-</sub> t <sub>2-3+</sub> t <sub>2-3-</sub> t <sub>14+12+</sub> t <sub>14-12-</sub> t <sub>14-3-</sub> t <sub>14-3+</sub> t <sub>13-12-</sub> t <sub>13-12+</sub> t <sub>13-3-</sub> t <sub>13-3+</sub>	12 12 3 3 12 12 3 3 12 3 3 3	- - - - - - - - - - - -	- - - - - - - - - - -	60 60 65 60 - 65 60 - - - -	- - - - - - - - - - -	ns ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓	- - - - - - - - - - -	- - - - - - - - - -	- - - - - - - - - -	- - - - - - - - - -	- - - - - - - - - -	60 60 65 60 - 65 60 - - -	- - - - - - - - - -	- - - - - - - - - -	ns ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓	Pulse In 2 ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓	Pulse Out 12 12 3 3 12 12 12 3 12 12 3 2,14 2,14	- - - - - - - - - - - -	11 ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓	4 ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓				

Ground Input pins of subtractor not under test. Other pins not listed are left open.

**MC797P, MC897P (continued)**



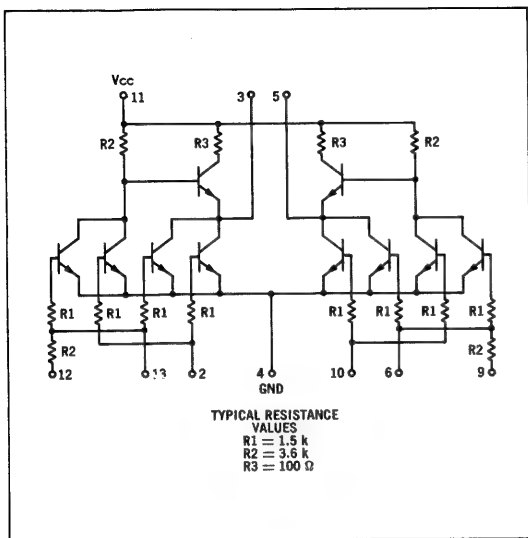
**SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS**



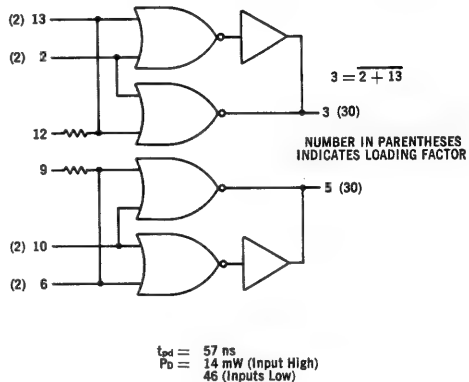
# DUAL 2-INPUT BUFFERS

PLASTIC mW MRTL MC700P/800P series

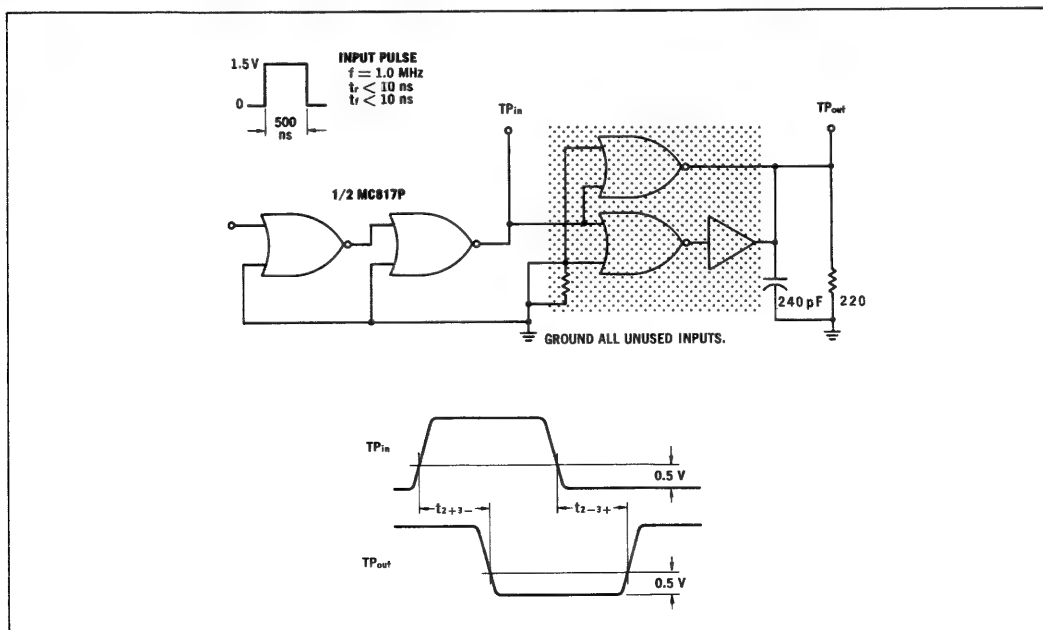
## MC798P • MC898P



Dual 2-input buffers designed to drive a greater number of loads than the basic Resistor Transistor Logic circuit. Returning an input resistor to  $V_{CC}$  allows for capacitive coupling in multivibrator and differentiator applications.



## SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



## ELECTRICAL CHARACTERISTICS

Test procedures are shown for one buffer only.  
The other buffer is tested in the same manner.

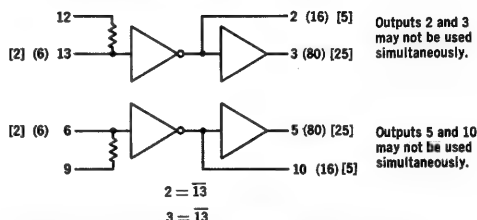
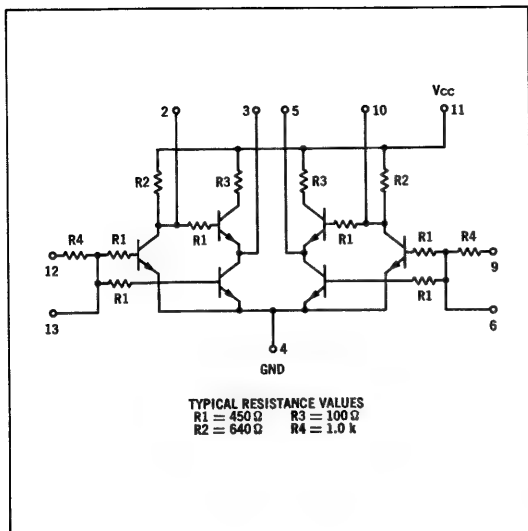
Characteristic	Symbol	Pin Under Test	MC898P Test Limits							MC798P Test Limits							TEST VOLTAGE							Gnd
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	APPLIED TO PINS LISTED BELOW:							
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		V <sub>in</sub>	V <sub>on</sub>	V <sub>BoT</sub>	V <sub>off</sub>	V <sub>CC</sub>	V <sub>R</sub> *		
Input Current	2 I <sub>In</sub>	2	-	300	-	280	-	280	μA <sub>dc</sub>	-	300	-	300	-	300	μA <sub>dc</sub>	2	-	13	-	11	-	4	
Output Current	I <sub>AB</sub>	3	4.5	-	4.5	-	4.5	-	mA <sub>dc</sub>	5.0	-	5.0	-	5.0	-	mA <sub>dc</sub>	-	3	-	2,13	11	-	4	
Output Voltage	V <sub>out</sub>	3	-	400	-	350	-	300	mV <sub>dc</sub>	-	400	-	300	-	320	mV <sub>dc</sub>	-	13	-	-	11	3	2,4	
		3	-	400	-	350	-	300	mV <sub>dc</sub>	-	400	-	300	-	320	mV <sub>dc</sub>	-	2	-	-	11	3	4,13	
Saturation Voltage	V <sub>CE(sat)</sub>	3	-	250	-	250	-	250	mV <sub>dc</sub>	-	220	-	230	-	320	mV <sub>dc</sub>	-	-	13	-	11	3	2,4	
		3	-	250	-	250	-	250	mV <sub>dc</sub>	-	220	-	230	-	320	mV <sub>dc</sub>	-	-	2	-	11	3	4,13	
Switching Time	t <sub>on</sub> + t <sub>off</sub>	2,3	-	-	-	160	-	-	ns	-	-	-	160	-	-	ns	Pulse In	Pulse Out	-	-	11	-	4,13	
																	2	3						

Ground input pins of buffer not under test. Other pins not listed are left open. \*Resistor value to V<sub>CC</sub>.

@ Test Temperature		TEST VOLTAGE VALUES						
		(Volts)					(k Ohms)	
		V <sub>IN</sub>	V <sub>ON</sub>	V <sub>BOT</sub>	V <sub>OFF</sub>	V <sub>CC</sub>	V <sub>R</sub> *	
MC898P	{	0°C	0.880	0.850	1.80	0.500	3.60	4.6
		+25°C	0.830	0.800	1.80	0.460	3.60	4.8
		+75°C	0.740	0.710	1.80	0.400	3.60	5.0
MC798P	{	+15°C	0.865	0.865	1.80	0.475	3.60	4.6
		+25°C	0.850	0.850	1.80	0.460	3.60	4.8
		+55°C	0.800	0.800	1.80	0.430	3.60	5.0

## PLASTIC MRTL MC700P/800P series

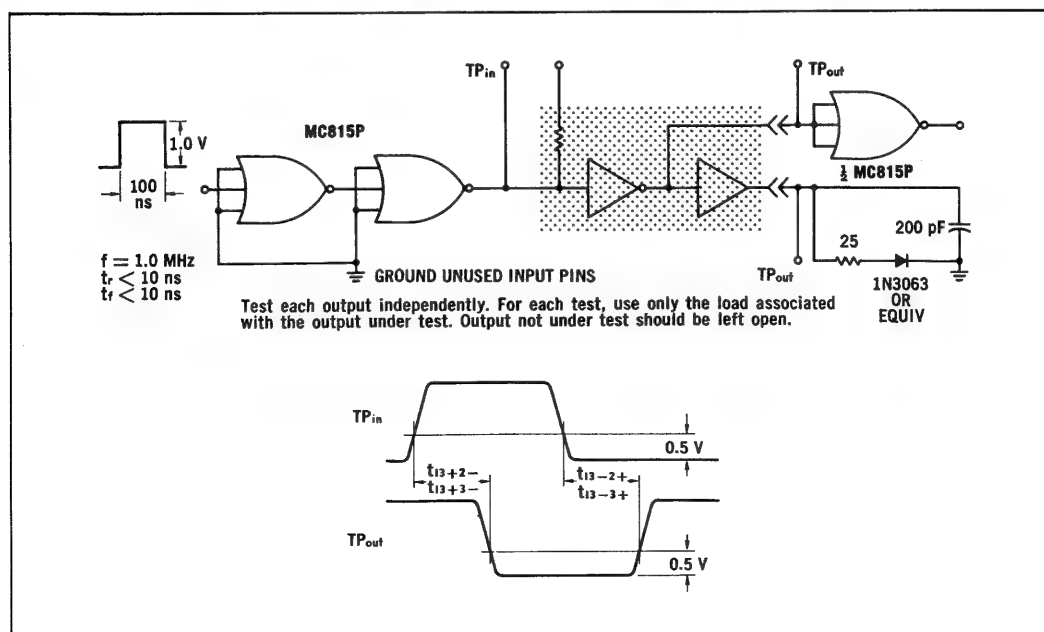
The dual buffer is designed to drive a greater number of load circuits than the basic RTL circuit. Because this circuit has a very low output impedance the rise times of output waveforms are maintained when driving capacitive loads. A resistor which is internally connected to the input allows for capacitive coupling to the input, the differentiation of input waveforms and various multivibrator applications.



NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL  
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL

$t_{pd} = 20 \text{ ns}$   
 $P_D = 50 \text{ mW}$  (Input High)  
 $100 \text{ mW}$  (Inputs Low)

### SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



## ELECTRICAL CHARACTERISTICS

Test procedures are shown for one buffer only.  
The other buffer is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC899P Test Limits							MC799P Test Limits							TEST VOLTAGE						Gnd
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	APPLIED TO PINS LISTED BELOW:						
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		Min	Max	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	
Input Current	2I <sub>In</sub>	13	-	1.2	-	1.2	-	1.1	mAdc	-	1.0	-	1.0	-	0.94	mAdc	13	-	-	-	11	-	4
Output Current	I <sub>A5</sub>	2	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	2	-	13	11	-	4
	I <sub>AB</sub>	3	15.0	-	15.0	-	14.25	-	mAdc	13.75	-	13.75	-	12.50	-	mAdc	-	3	-	13	11	-	4
Output Voltage	V <sub>out</sub>	2	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-	11	-	4
		3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-	11	3	4
Saturation Voltage	V <sub>CE(sat)</sub>	2	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	13	-	11	-	4
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	11, 12	-	↓
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	13	-	11	3	↓
Switching Time	t	13+3-	-	-	-	30	-	-	ns	-	-	-	30	-	-	ns	Pulse In	Pulse Out	-	-	11	-	4
		13-3+	-	-	-	45	-	-	↓	-	-	-	45	-	-	↓	13	3					
		13+2-	-	-	-	28	-	-	↓	-	-	-	28	-	-	↓	13	3					
		13-2+	-	-	-	32	-	-	↓	-	-	-	32	-	-	↓	13	2					
			-	-	-		-	-	↓	-	-	-		-	-	↓	13	2					

Ground all unused input pins. Other pins not listed are left open. \* Resistor Value to V<sub>CC</sub>

@ Test

Temperature

MC899P { 0°C  
+25°C  
+75°C  
MC799P { +15°C  
+25°C  
+55°C

## TEST VOLTAGE VALUES

(Volts)

(Ohms)

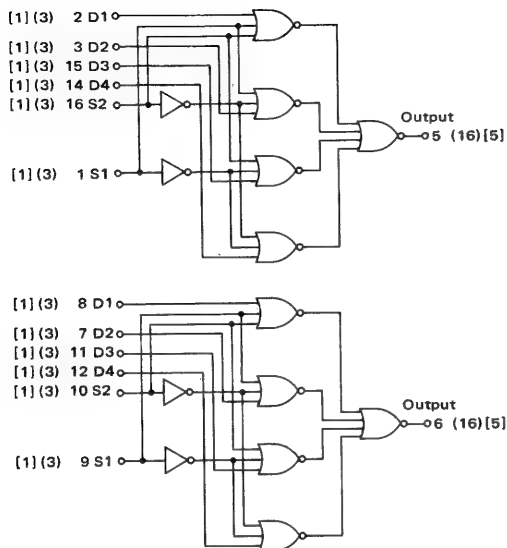
V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	V <sub>R</sub> *
0.960	0.930	1.80	0.570	3.60	640
0.910	0.800	1.80	0.500	3.60	640
0.820	0.790	1.80	0.450	3.60	750
0.865	0.865	1.80	0.475	3.60	640
0.850	0.850	1.80	0.460	3.60	640
0.800	0.800	1.80	0.430	3.60	640

# DUAL 4-CHANNEL DATA SELECTOR/MULTIPLEXER

PLASTIC MRTL MC700P/800P series

MC9701P • MC9801P

A dual electronic four-position switch that enables selection of any one of four data input lines selected by a binary coded select input.



TRUTH TABLE

Input Select		Data Line Selected
S1	S2	
0	0	D1
0	1	D2
1	0	D3
1	1	D4

$$\text{Output} = \overline{S1} \overline{S2} D1 + \overline{S1} S2 D2 + S1 \overline{S2} D3 + S1 S2 D4$$

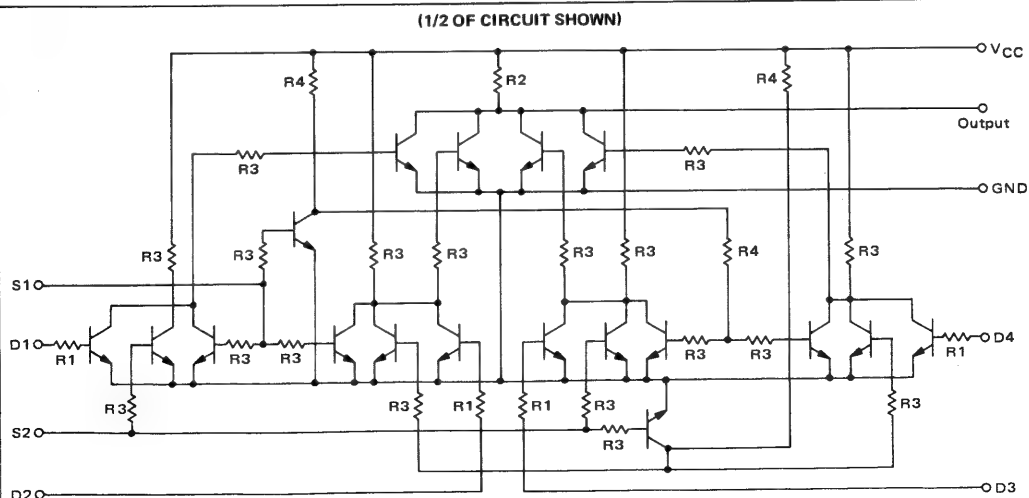
$$\text{Avg. } t_{pd} = 25 \text{ ns typ} \quad \text{Avg. } t_{pd} = \frac{t_{++} + t_{--}}{2}$$

$$P_D = 100 \text{ mW typ}$$

$$\text{Operating Frequency} = 18 \text{ MHz typ}$$

(Both Selector Inputs and Data Inputs High)

Number in Parenthesis Indicates mW MRTL Loading Factor.  
Number in Brackets Indicates MRTL Loading Factor.



TYPICAL RESISTANCE VALUES

$$R1 = 450 \Omega$$

$$R3 = 1.5 \text{ k}$$

$$R2 = 640 \Omega$$

$$R4 = 3.6 \text{ k}$$

# ELECTRICAL CHARACTERISTICS

Test procedures are shown for one data selector only. The other data selector is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC9801P Test Limits							MC9701P Test Limits							TEST VOLTAGE APPLIED TO PINS LISTED BELOW:				
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	V <sub>In</sub>	V <sub>on</sub>	V <sub>off</sub>	V <sub>CC</sub>	Gnd
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max						
Input Current	I <sub>In</sub>	1 2 3 14 15 16	- 600 - - - ↓	600 - - - - ↓	- 600 - - - ↓	- - - - - ↓	570 - - - - ↓	μA <sub>dc</sub> - - - - ↓	- 500 - - - ↓	- - - - - ↓	500 - - - - ↓	- - - - - ↓	470 - - - - ↓	μA <sub>dc</sub> - - - - ↓	1 2 3 14 15 16	- - - - - -	- - - - - -	13 - - - - ↓	4 - - - - ↓		
Output Current	I <sub>A5</sub>	5 5 5 5	-3.0 - - ↓	- - - -	-3.0 - - ↓	- - - -	-2.85 - - ↓	- - - -	mA <sub>dc</sub> - - ↓	-2.65 - - ↓	- - - -	-2.65 - - ↓	- - - -	-2.5 - - ↓	- - - -	mA <sub>dc</sub> - - ↓	- - - -	2,5 3,5,16 1,5,14,16 1,5,15	1,16 1 - 16	13 - - ↓	4 - - ↓
Saturation Voltage	V <sub>CE(sat)</sub>	5 5 5 5	- - - ↓	400 - - ↓	- - - ↓	400 - - ↓	- - - ↓	400 - - ↓	mV <sub>dc</sub> - - ↓	- - - ↓	300 - - ↓	- - - ↓	300 - - ↓	- - - ↓	320 - - ↓	mV <sub>dc</sub> - - ↓	- - - -	- 16 1 1,16	1,2,16 1,3 15,16 14	13 - - ↓	4 - - ↓
Power Supply Current Drain	I <sub>PD</sub> *	13	-	-	-	37	-	-	mA <sub>dc</sub>	-	-	-	37	-	-	mA <sub>dc</sub>	1,9,10,16	-	-	-	-
Switching Times	t <sub>2+5+</sub> t <sub>2-5-</sub>	5	-	-	-	32	-	-	ns	-	-	-	32	-	-	ns	Pulse In	Pulse Out	-	13	1,4,16 1,4,16
		5	-	-	-	26	-	-	ns	-	-	-	26	-	-	ns	2	5			
		5	-	-	-	26	-	-	ns	-	-	-	26	-	-	ns	2	5			

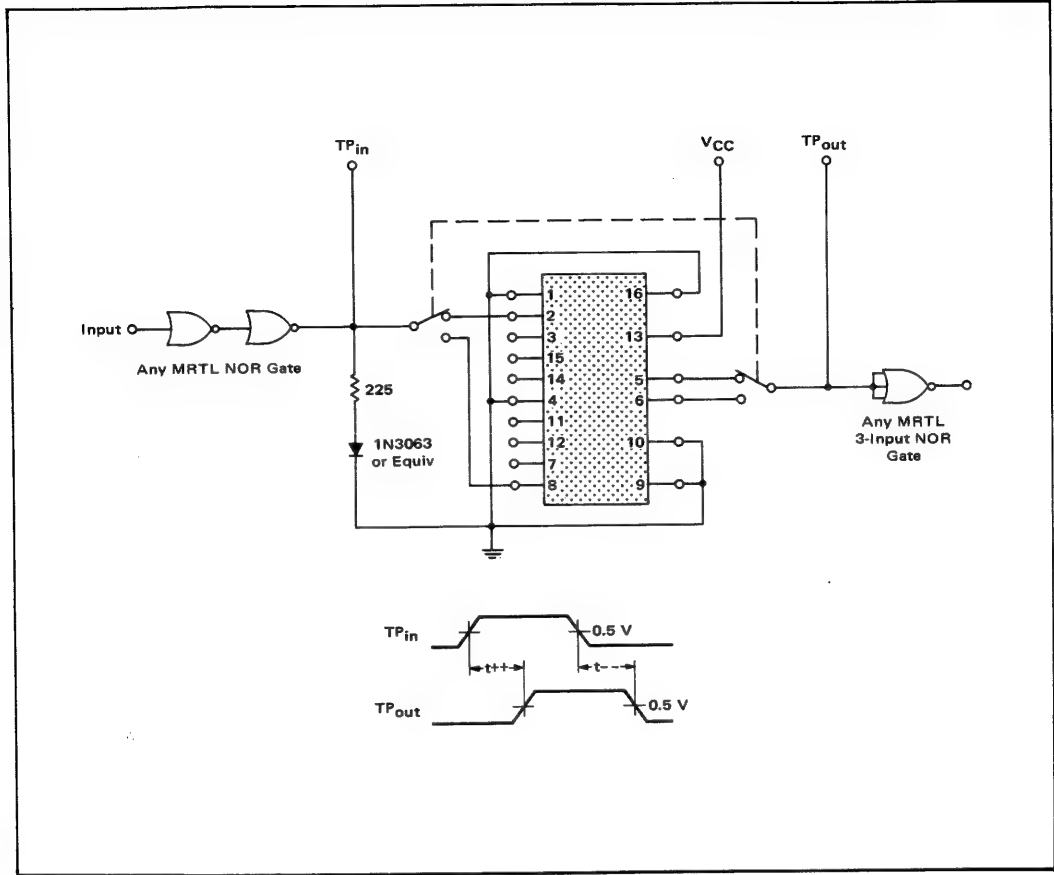
\*I<sub>PD</sub> test is for both halves of the dual selector.

Ground inputs of dual selector not under test. Other pins not listed are left open.

@ Test Temperature  
MC9801P { 0°C  
+25°C  
+75°C  
MC9701P { +15°C  
+25°C  
+55°C



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

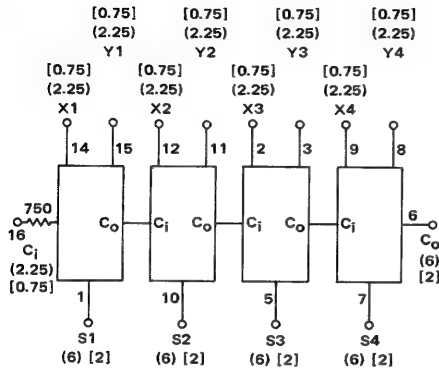


4-BIT PARALLEL  
FULL ADDER

PLASTIC MRTL MC700P/800P series

MC9704P • MC9804P

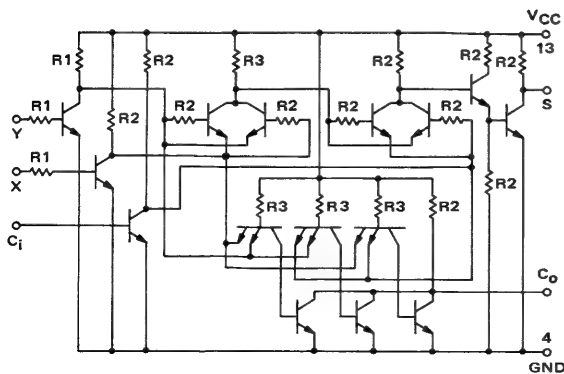
MC9704P/9804P is a four-bit full adder with ripple-through carry.



$C_o t_{pd} = 125 \text{ ns typ}$   
 $P_D = 265 \text{ mW typ}$   
 Operating Frequency = 8.0 MHz

Number in Parenthesis Indicates Loading Factor for mW MRTL. Number in Brackets Indicates Loading Factor for MRTL.

(1/4 OF CIRCUIT SHOWN)



TYPICAL RESISTANCE VALUES  
 $R1 = 750 \Omega$   
 $R2 = 1.5 \text{ k}$   
 $R3 = 3.6 \text{ k}$

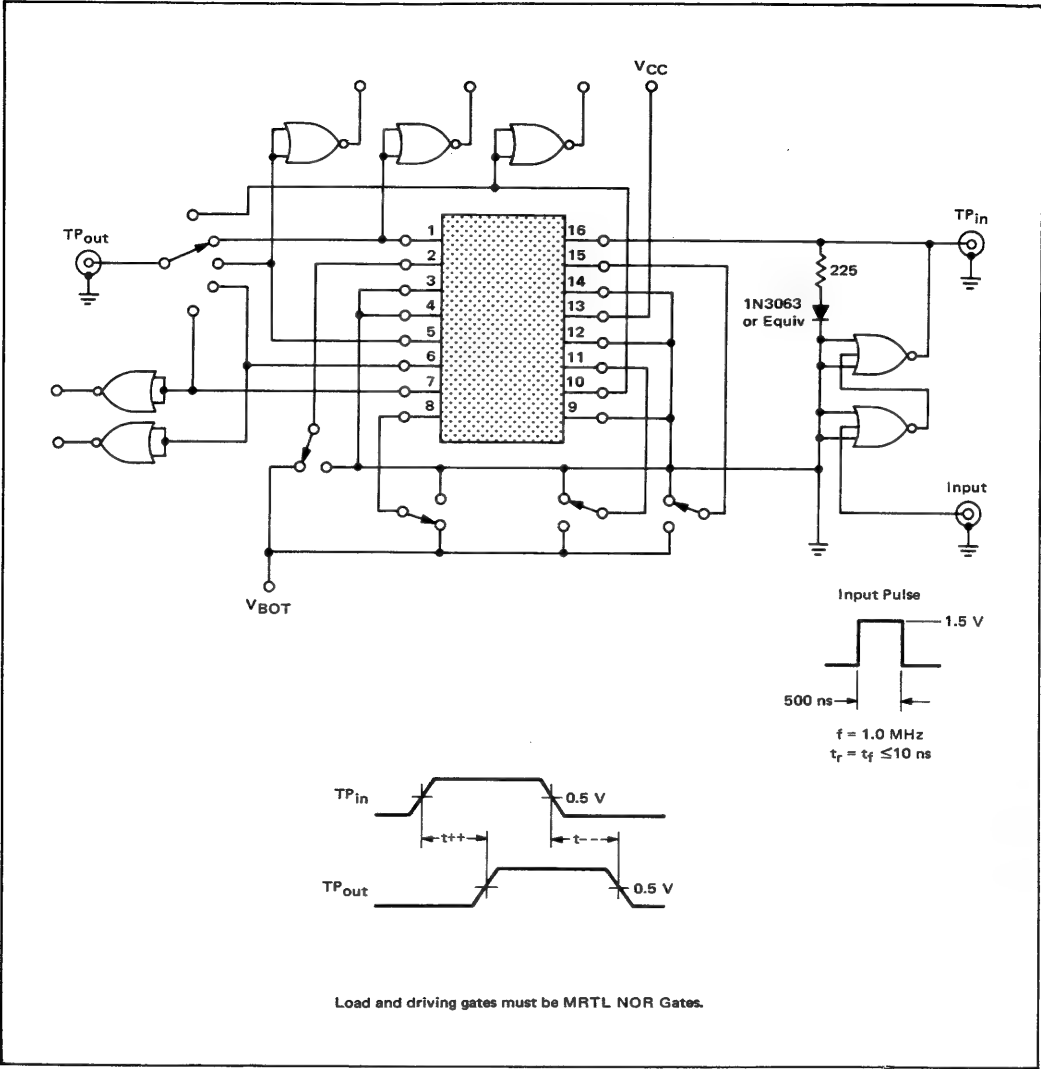
## ELECTRICAL CHARACTERISTICS

Test procedures are shown for one adder only. The other adders are tested in the same manner.

ELECTRICAL CHARACTERISTICS											TEST VOLTAGE VALUES																							
Test procedures are shown for one adder only. The other adders are tested in the same manner.											(Volts)																							
											@ Test Temperature																							
											V <sub>in</sub> V <sub>on</sub> V <sub>BOT</sub> V <sub>off</sub> V <sub>CC</sub>																							
											0°C																							
MC9804P											+25°C																							
											+75°C																							
MC9704P											+15°C																							
											+25°C																							
											+55°C																							
											0.960 0.930 1.80 0.570 3.60																							
											0.910 0.880 1.80 0.500 3.60																							
											0.820 0.790 1.80 0.450 3.60																							
											0.865 0.865 1.80 0.475 3.60																							
											0.850 0.850 1.80 0.460 3.60																							
											0.800 0.800 1.80 0.430 3.60																							
Characteristic											TEST VOLTAGE APPLIED TO PINS LISTED BELOW:											Gnd												
Symbol											V <sub>in</sub> V <sub>on</sub> V <sub>BOT</sub> V <sub>off</sub> V <sub>CC</sub>																							
Pin Under Test																																		
MC9804P Test Limits											MC9704P Test Limits																							
0°C +25°C +75°C											+15°C +25°C +55°C																							
Min Max Min Max Min Max											Min Max Min Max Min Max																							
Unit											Unit																							
Input Current											14 15 16											13	4											
Output Current											1 5 6 7 10											13	4											
Output Voltage											1 5 6 7 10											13	4											
Power Supply Current Drain											13											13	4											
Switching Times Propagation Delay											t <sub>16+6+</sub> t <sub>16-6-</sub> t <sub>16+1+</sub> t <sub>16-1-</sub> t <sub>16+10+</sub> t <sub>16-10-</sub> t <sub>16+5+</sub> t <sub>16-5-</sub> t <sub>16+7+</sub> t <sub>16-7-</sub>											Pulse In Pulse Out											13	3,4,9,12,14

Pins not listed are left open.

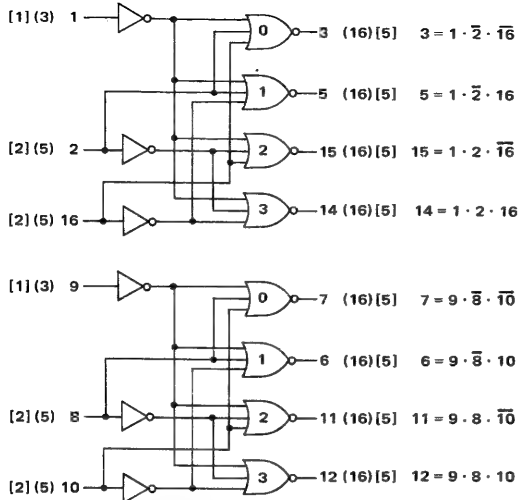
SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



DUAL 4-CHANNEL  
DATA DISTRIBUTOR

PLASTIC MRTL MC700P/800P series

MC9707P • MC9807P†



Number in parenthesis indicates loading factor for mW MRTL.  
Number in brackets indicates loading factor for MRTL.

MC9707P/MC9807P consists of two electronic, one-pole, four-position switches which route one-bit of binary data to one of four output lines. Switching is accomplished by means of a pair of BCD coded select lines.

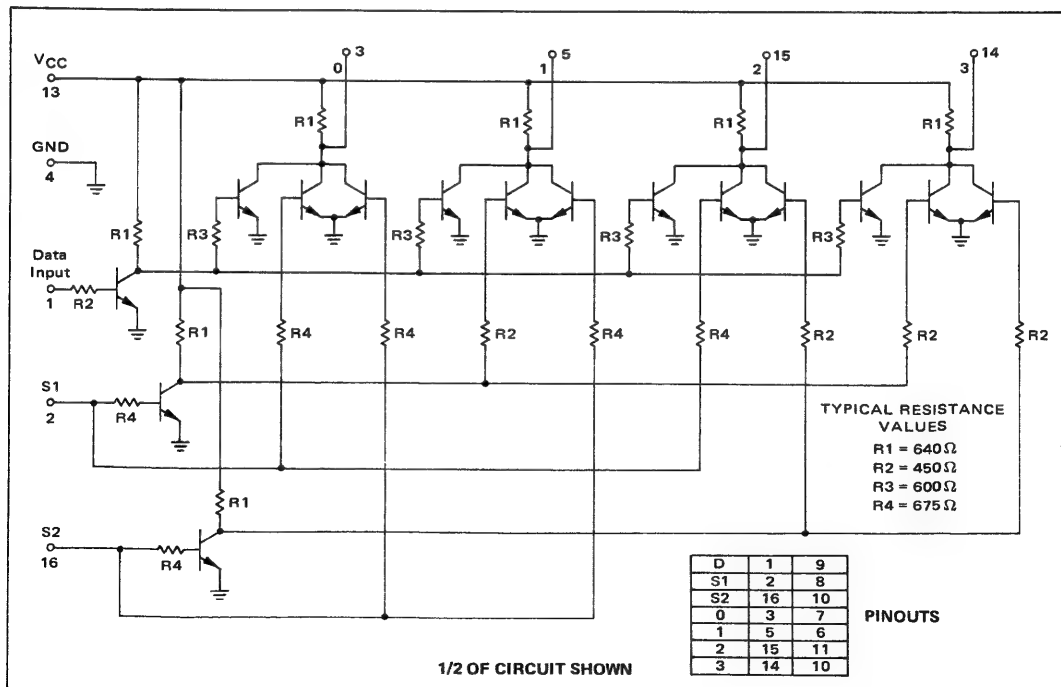
TRUTH TABLE

		INPUTS		OUTPUTS			
		D	S1 S2	0	1	2	3
Pin	Numbers	1	2 16	3	5	15	14
Level		9	8 10	7	6	11	12
0	*	*	0 0	0	0	0	0
1	0	0	1 0	0	0	0	0
1	0	1	0 1	0	1	0	0
1	1	0	0 0	0	0	1	0
1	1	1	0 0	0	0	0	1

\*Either state.

$A_{vg}^* t_{pd} = 25 \text{ ns typ}$   
 $P_D = 150 \text{ mW typ}$

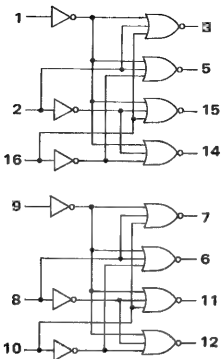
$$^* A_{vg} t_{pd} = \frac{t_{on} + t_{off}}{2}$$



†See General Information section for packaging.

# ELECTRICAL CHARACTERISTICS

Test procedures are given for only one of the Dual Data Distributors. The other Data Distributor is tested in the same manner.



@ Test  
Temperature

MC9807P { 0°C  
+25°C  
+75°C

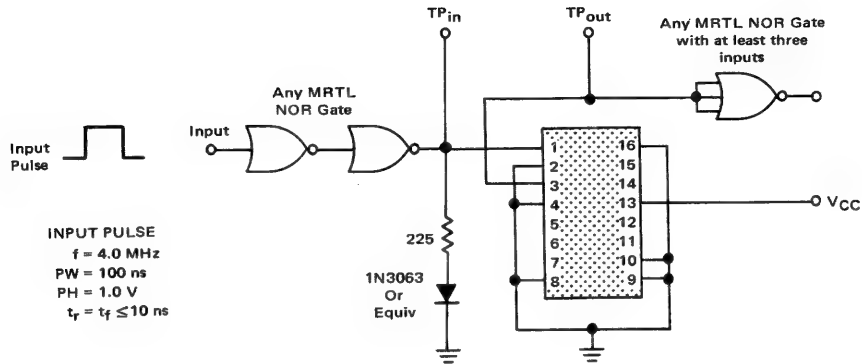
MC9707P { +15°C  
+25°C  
+55°C

TEST VOLTAGE VALUES					
(Volts)					
V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	
0.960	0.930	1.80	0.570	3.60	
0.910	0.880	1.80	0.500	3.60	
0.820	0.790	1.80	0.450	3.60	
0.865	0.865	1.80	0.475	3.60	
0.850	0.850	1.80	0.460	3.60	
0.800	0.800	1.80	0.430	3.60	
TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					
V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	Gnd
1	-	-	-	13	4
2	-	16	-	↓	↓
16	-	1	-	↓	↓
-	1,3	-	2,16	13	4
-	1,5,16	-	2	↓	↓
-	1,2,14,16	-	-	↓	↓
-	1,2,15	-	16	↓	↓
-	2	1	-	13	4,16
-	2	1,16	-	↓	4
-	2,16	1	-	↓	↓
-	16	1,2	-	↓	↓
-	-	2,8,10,16	-	13	1,4,9
Pulse In	Pulse Out				
1	3	-	-	13	2,16
1	3	-	-	13	2,16

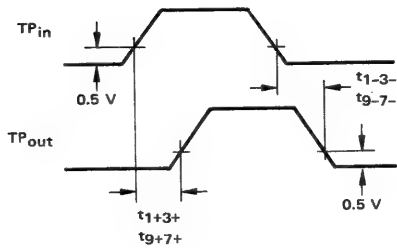
Characteristic	Symbol	Pin Under Test	MC9807P Test Limits							Unit	MC9707P Test Limits						
			0°C		+25°C		+75°C		Unit		+15°C		+25°C		+55°C		Unit
			Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
Input Current	I <sub>in</sub>	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	
	2 <sub>in</sub>	2 16	-	1200 1200	-	1200 1200	-	1140 1140	↓	-	1000 1000	-	1000 1000	-	940 940	↓	
Output Current	I <sub>A5</sub>	3	3.00	-	3.00	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	
		5															
		14															
		15	↓	-	↓	-	-	-	↓	↓	-	↓	-	↓	-	↓	
Output Voltage	V <sub>out</sub>	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	
		5	-		-		-			-		-		-			
		14	-		-		-			-		-		-			
		15	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	
Power Supply Drain Current	I <sub>PD</sub>	13	-	-	-	68	-	-	mAdc	-	-	-	68	-	-	mAdc	
Switching Times	t <sub>1+3+</sub>	1	-	-	-	36	-	-	ns	-	-	-	36	-	-	ns	
	t <sub>1-3-</sub>	1	-	-	-	26	-	-	ns	-	-	-	26	-	-	ns	

Ground input pins of data distributor not under test.  
Other pins not listed are left open.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



To measure  $t_{g+7+}$  and  $t_{g-7-}$ , connect input to pin 9, output to pin 7, and ground pin 1. The remainder of the test configuration is unchanged.

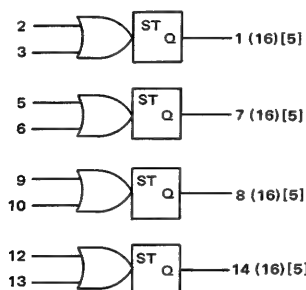


QUAD SCHMITT  
TRIGGER

PLASTIC MRTL MC700P/800P series

MC9709P • MC9809P

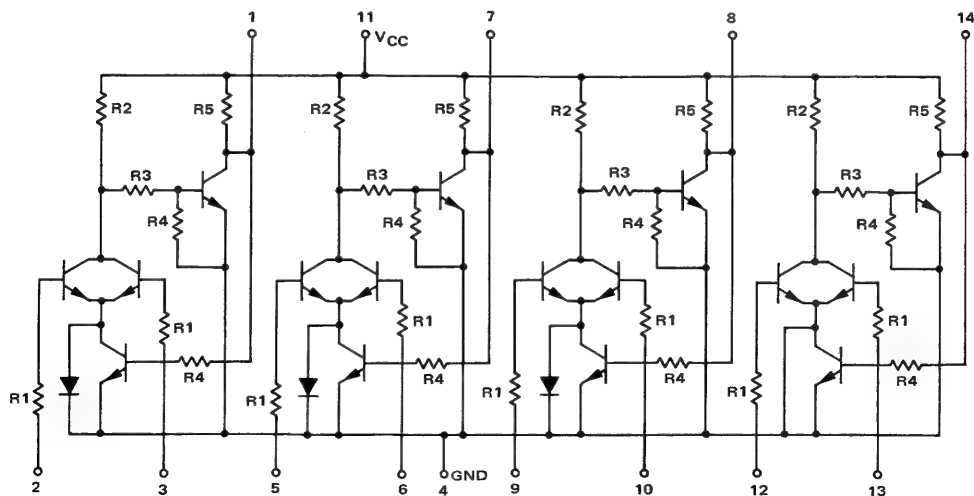
The MC9709P/9809P device consists of four Schmitt Triggers in a single 14-pin dual in-line plastic package. It provides a square-wave output from a slow-rise-time input with 650 mV internal hysteresis.



$t_r = t_f = 20 \text{ ns typ}$   
 Avg.  $t_{pd} = 30 \text{ ns typ}$ , Avg.  $= \frac{t_{on} + t_{off}}{2}$   
 $f = 18 \text{ MHz typ}$   
 $P_D = 95 \text{ mW typ}$

Upper Trigger Voltage = 1.40 V typ  
 Lower Trigger Voltage = 0.75 V typ

Number in Parenthesis Indicates mW MRTL Loading Factor.  
 Number in Brackets Indicates MRTL Loading Factor.



TYPICAL RESISTANCE VALUES  
 $R1 = 450 \Omega$        $R4 = 1.5 \text{ k}$   
 $R2 = 2.0 \text{ k}$        $R5 = 640 \Omega$   
 $R3 = 500 \Omega$



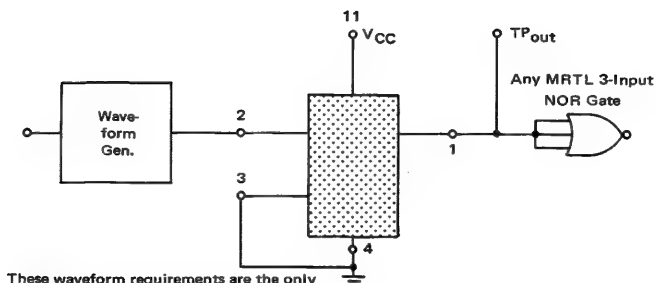
**ELECTRICAL CHARACTERISTICS**

Test procedures are shown for one Schmitt Trigger only. The other Schmitt triggers are tested in the same manner.

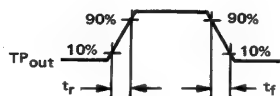
ELECTRICAL CHARACTERISTICS																	TEST VOLTAGE VALUES				Gnd
<p>Test procedures are shown for one Schmitt Trigger only. The other Schmitt triggers are tested in the same manner.</p> <div><div>@ Test Temperature</div><div><div>MC9809P</div><div>0°C</div><div>+25°C</div><div>+75°C</div></div><div><div>MC9709P</div><div>+15°C</div><div>+25°C</div><div>+55°C</div></div></div>																	(Volts)				
																	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	
																	0.930	1.80	0.570	3.60	
																	0.880	1.80	0.500	3.60	
																	0.790	1.80	0.450	3.60	
																	0.865	1.80	0.475	3.60	
																	0.850	1.80	0.460	3.60	
																	0.800	1.80	0.430	3.60	
Characteristic	Symbol	Pin Under Test	MC9809P Test Limits							MC9709P Test Limits							TEST VOLTAGE APPLIED TO PINS LISTED BELOW:				
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max						
Output Current	I <sub>A5</sub>	1 1	3.0 3.0	-	3.0 3.0	-	2.85 2.85	-	mAdc	2.65 2.65	-	2.65 2.65	-	2.50 2.50	-	mAdc mAdc	1 1	2 3	- -	11 11	
Output Voltage	V <sub>out</sub>	1	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	-	2,3	11	
Power Supply Drain Current (Total Device)	I <sub>PD</sub>	11	-	-	-	32	-	-	mAdc	-	-	-	32	-	-	mAdc	-	-	-	11	
Output Pulse	t <sub>1+</sub>	1	-	100	-	100	-	100	ns	-	100	-	100	-	100	ns	Pulse Out 1	Input 2	-	11	
Rise and Fall Times	t <sub>1-</sub>	1	-	100	-	100	-	100	ns	-	100	-	100	-	100	ns	1	2	-	11	

Ground unused input pins. Other pins not listed are left open.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



These waveform requirements are the only restrictions for test.  
 $f \geq 60 \text{ Hz}$   
 $P_A^* = 2.0 \text{ V}$  \*Do not exceed  $\pm 4.0$  volts.

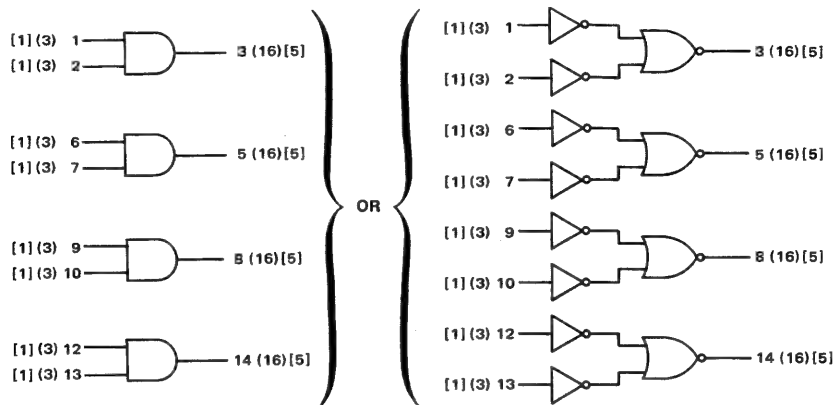


QUAD 2-INPUT  
"AND" GATE

PLASTIC MRTL MC700P/800P series

MC9713P • MC9813P

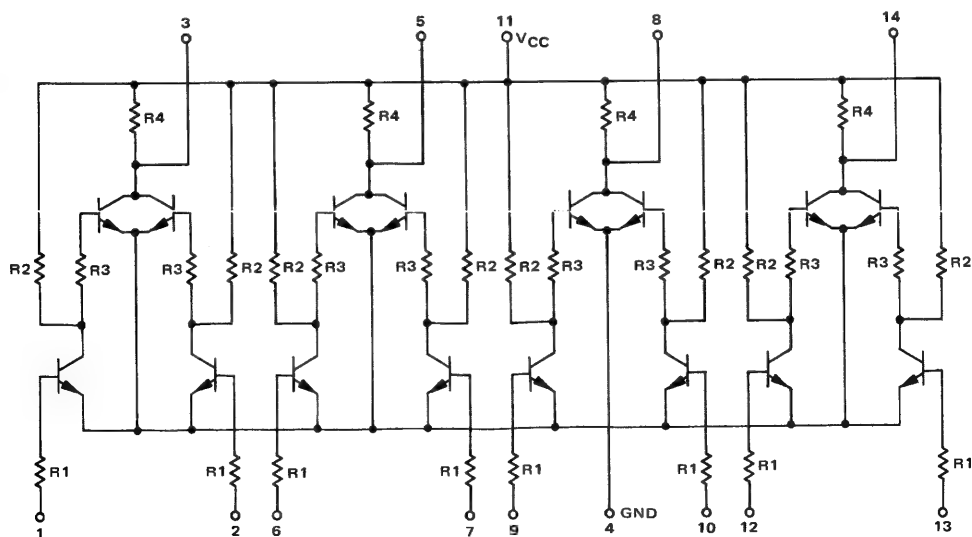
Increased logic flexibility is provided by MC9713P/9813P, quad 2-input AND gates in a single 14-pin dual in-line plastic package.



Number In Parenthesis Indicates Loading Factor For mW MRTL.  
Number In Brackets Indicates Loading Factor For MRTL.

Avg  $t_{pd}^* = 28 \text{ ns typ}$   
 $P_D = 100 \text{ mW typ}$   
Operating  $f = 14 \text{ MHz typ}$

$$^* \text{Avg } t_{pd} = \frac{t_{on} + t_{off}}{2}$$



TYPICAL RESISTANCE VALUES  
R1 = 450  $\Omega$       R3 = 1.5 k  
R2 = 1.8 k      R4 = 640  $\Omega$

# ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only. The other gates are tested in the same manner.

@ Test Temperature				TEST VOLTAGE VALUES					Gnd
				(Volts)					
				V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	
MC9813P	0°C			0.960	0.930	1.80	0.570	3.60	
	+25°C			0.910	0.880	1.80	0.500	3.60	
	+75°C			0.820	0.790	1.80	0.450	3.60	
MC9713P	+15°C			0.865	0.865	1.80	0.475	3.60	
	+25°C			0.850	0.850	1.80	0.460	3.60	
	+55°C			0.800	0.800	1.80	0.430	3.60	
Test Limits				TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					Gnd
	+55°C		Unit	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	
x	Min	Max							
0	-	470	μAdc	1	-	-	-	11	4
0	-	470	μAdc	2	-	-	-	11	4
	2.50	-	mAdc	-	1,2,3	-	-	11	4
0	-	320	mVdc	-	2	-	1	11	4
0	-	320	mVdc	-	1	-	2	11	4
3	-	-	mAdc	-	-	2,7,10,13	-	11	1,4,6,9,12
				Pulse In	Pulse Out				
	-	-	ns	1	3	2	-	11	4
6	-	-		1		2	-		
2	-	-		2		1	-		
3	-	-	↓	2	↓	1	-	↓	↓

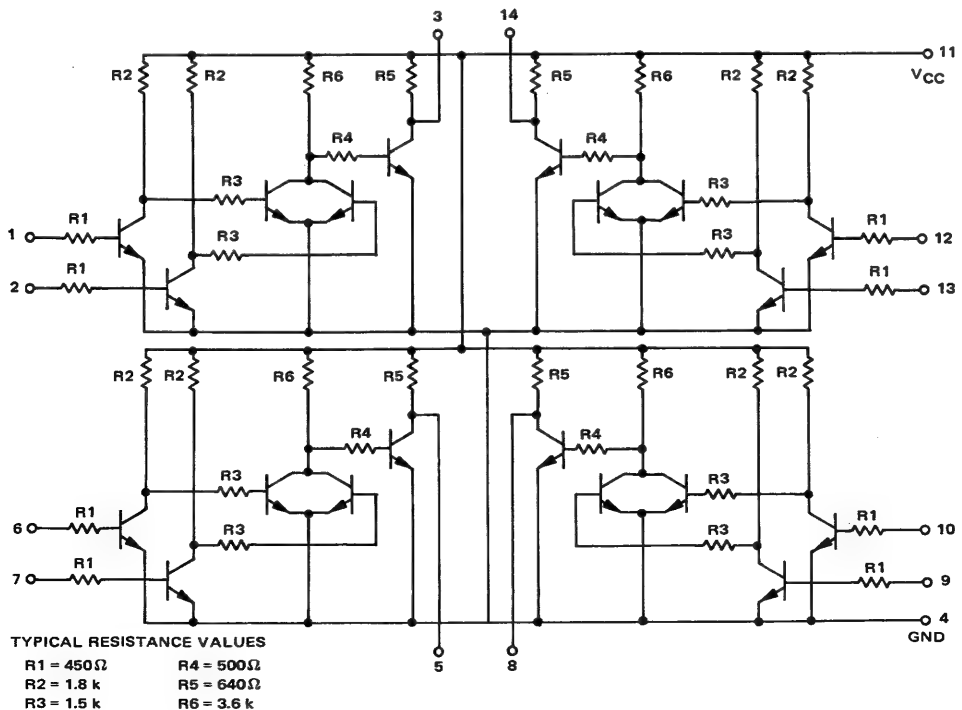
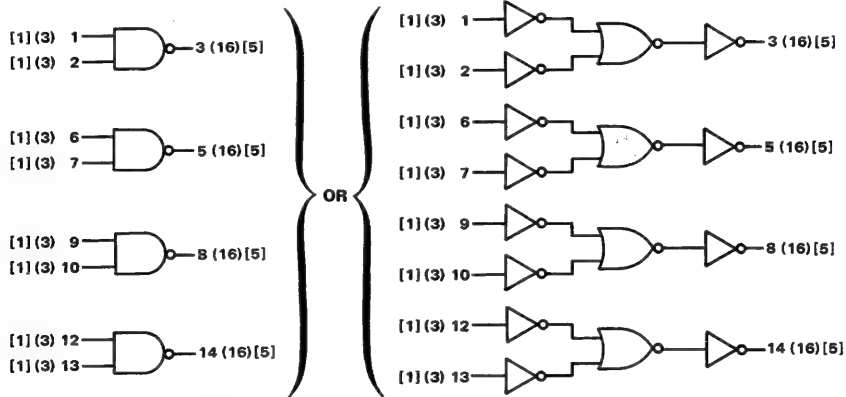


QUAD 2-INPUT  
"NAND" GATE

PLASTIC MRTL MC700P/800P series

## MC9714P • MC9814P

Increased logic flexibility is provided by MC9714P/9814P, quad 2-input positive logic NAND gates in a single 14-pin dual in-line plastic package.



# ELECTRICAL CHARACTERISTICS

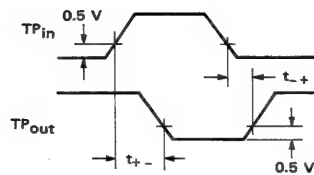
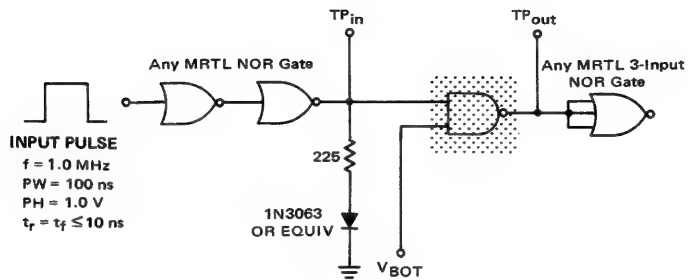
Test procedures are shown for one gate only. The other gates are tested in the same manner.

ELECTRICAL CHARACTERISTICS																	TEST VOLTAGE VALUES					Gnd
																	(Volts)					
																	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	
																	@ Test Temperature					
																	MC9814P					
																	0°C	+25°C	+75°C			
																	0.960	0.930	1.80	0.570	3.60	
																	0.910	0.880	1.80	0.500	3.60	
																	0.820	0.790	1.80	0.450	3.60	
																	0.865	0.865	1.80	0.475	3.60	
																	0.850	0.850	1.80	0.460	3.60	
																	0.800	0.800	1.80	0.430	3.60	
																	TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					
																	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	
Characteristic	Symbol	Pin Under Test	MC9814P Test Limits						Unit	MC9714P Test Limits						Unit						
			0°C		+25°C		+75°C				+15°C		+25°C		+55°C			V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>
Input Current	I <sub>in</sub>	1	-	600	-	600	-	570	μA <sub>dc</sub>	-	500	-	500	-	470	μA <sub>dc</sub>	1	-	-	-	11	4
		2	-	600	-	600	-	570	μA <sub>dc</sub>	-	500	-	500	-	470	μA <sub>dc</sub>	2	-	-	-	11	4
Output Current	I <sub>A5</sub>	3	3.0	-	3.0	-	2.85	-	mA <sub>dc</sub>	2.65	-	2.65	-	2.50	-	mA <sub>dc</sub>	-	2,3	-	1	11	4
		3	3.0	-	3.0	-	2.85	-	mA <sub>dc</sub>	2.65	-	2.65	-	2.50	-	mA <sub>dc</sub>	-	1,3	-	2	11	4
Output Voltage	V <sub>out</sub>	3	-	400	-	300	-	350	mV <sub>dc</sub>	-	300	-	290	-	320	mV <sub>dc</sub>	-	1,2	-	-	11	4
Power Supply Drain Current	I <sub>PD</sub> *	11	-	-	-	52	-	-	mA <sub>dc</sub>	-	-	-	52	-	-	mA <sub>dc</sub>	-	-	1,2,6,7,9,10,12,13	-	11	4
Switching Times	t <sub>1+3-</sub> t <sub>1-3+</sub> t <sub>2+3-</sub> t <sub>2-3+</sub>	3	-	-	-	57	-	-	ns	-	-	-	57	-	-	ns	Pulse In	Pulse Out	2	-	11	4
		↓	-	-	-	38	-	-	↓	-	-	-	38	-	-	↓	1	3	2	-	↓	↓
		↓	-	-	-	57	-	-	↓	-	-	-	57	-	-	↓	2	3	1	-	↓	↓
		↓	-	-	-	38	-	-	↓	-	-	-	38	-	-	↓	2	3	1	-	↓	↓
		↓	-	-	-	38	-	-	↓	-	-	-	38	-	-	↓	2	3	1	-	↓	↓

Ground inputs of gates not under test. Pins not listed are left open.

\*This test includes all gates (13 mA<sub>dc</sub> per gate).

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



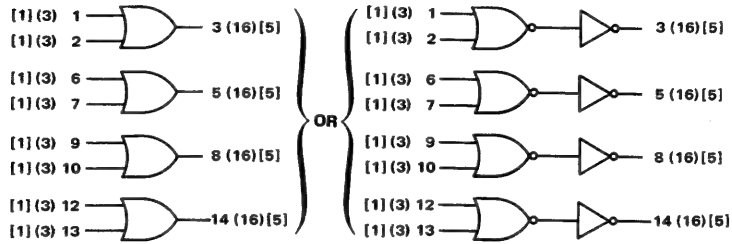


QUAD 2-INPUT  
"OR" GATE

PLASTIC MRTL MC700P/800P series

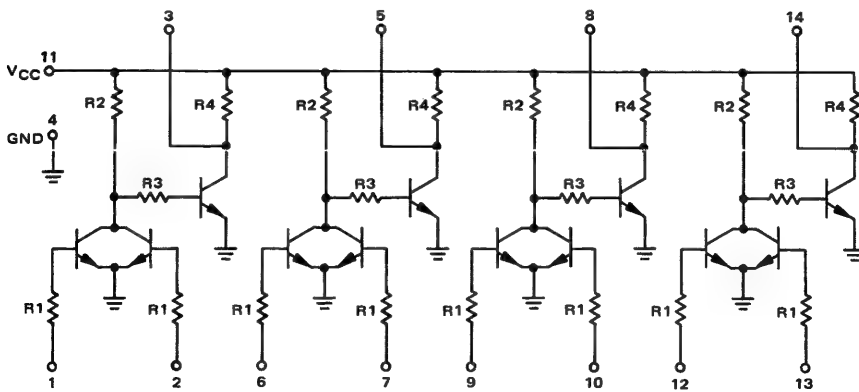
## MC9715P • MC9815P

MC9715P/9815P provides increased logic flexibility, quad 2-input OR gates housed in a single 14-pin dual in-line plastic package.



$P_D = 100 \text{ mW typ (Inputs Low)}$   
 $= 28 \text{ mW typ (Inputs High)}$   
 Operating  $f = 14 \text{ MHz typ}$

Number In Parenthesis Indicates mWMRTL Loading Factor.  
 Number In Brackets Indicates MRTL Loading Factor.



### TYPICAL RESISTANCE VALUES

$R1 = 450 \Omega$        $R3 = 500 \Omega$   
 $R2 = 1.8 \text{ k}$        $R4 = 640 \Omega$

## ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner.

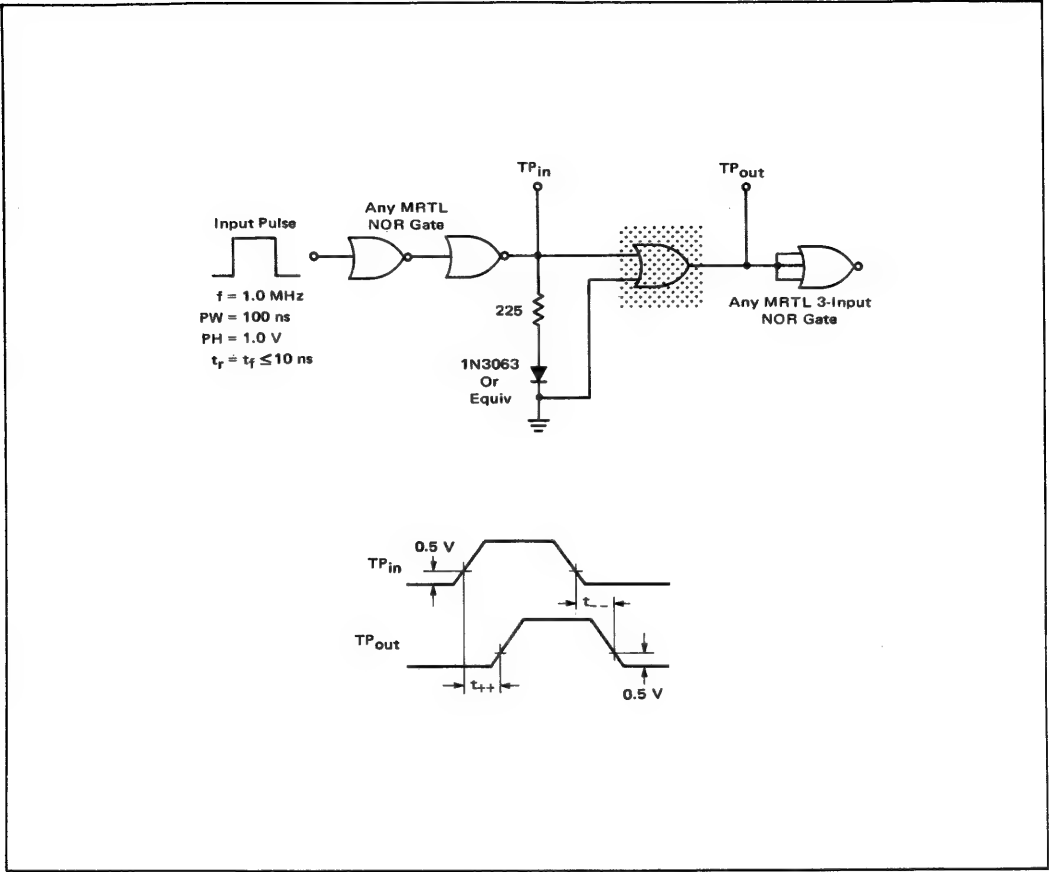
ELECTRICAL CHARACTERISTICS										<div>@ Test Temperature</div> <div>MC9815P { +0°C +25°C +75°C MC9715P { +15°C +25°C +55°C</div>										TEST VOLTAGE VALUES						Gnd
						(Volts)																				
V <sub>In</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>																						
0.960	0.930	1.80	0.570	3.60																						
										0.910	0.880	1.80	0.500	3.60												
										0.820	0.790	1.80	0.450	3.60												
										0.865	0.865	1.80	0.475	3.60												
										0.850	0.850	1.80	0.460	3.60												
										0.800	0.800	1.80	0.430	3.60												
Characteristic	Symbol	Pin Under Test	MC9815P Test Limits							MC9715P Test Limits							TEST VOLTAGE APPLIED TO PINS LISTED BELOW:									
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	V <sub>In</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>					
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max											
Input Current	I <sub>In</sub>	1 2	-	600 600	-	600 600	-	570 570	μA <sub>Dc</sub>	-	500 500	-	500 500	-	470 470	μA <sub>Dc</sub>	1 2	-	2 1	-	11 11	4 4				
Output Current	I <sub>A5</sub>	3	3.0	-	3.0	-	2.85	-	mA <sub>Dc</sub>	2.65	-	2.65	-	2.50	-	mA <sub>Dc</sub>	-	1,3	-	-	11	4				
Output Voltage	V <sub>out</sub>	3	-	400	-	300	-	350	mV <sub>Dc</sub>	-	300	-	290	-	320	mV <sub>Dc</sub>	-	-	-	1,2	11	4				
Power Supply Drain Current	I <sub>PD1</sub>	11	-	-	-	9.5	-	-	mA <sub>Dc</sub>	-	-	-	9.5	-	-	mA <sub>Dc</sub>	-	-	*	-	11	4				
	I <sub>PD2</sub>	11	-	-	-	33	-	-	mA <sub>Dc</sub>	-	-	-	33	-	-	mA <sub>Dc</sub>	-	-	-	-	11	4**				
Switching Times	t <sub>1+3+</sub> t <sub>1-3-</sub> t <sub>2+3+</sub> t <sub>2-3-</sub>	3 ↓	-	-	-	50	-	-	ns ↓	-	-	-	50	-	-	ns ↓	Pulse In	Pulse Out	-	-	11	2,4				
			-	-	-	45	-	-	-	45	-	-	-	45	-	-	-	-	-	-	2,4					
			-	-	-	50	-	-	-	50	-	-	-	50	-	-	-	-	-	-	1,4					
			-	-	-	45	-	-	-	45	-	-	-	45	-	-	-	-	-	-	↓	1,4				

Ground unused input pins. Other pins not listed are left open.

\*All inputs at V<sub>BOT</sub> (inputs 1, 2, 6, 7, 9, 10, 12, 13).

\*\*All inputs at ground (inputs 1, 2, 6, 7, 9, 10, 12, 13).

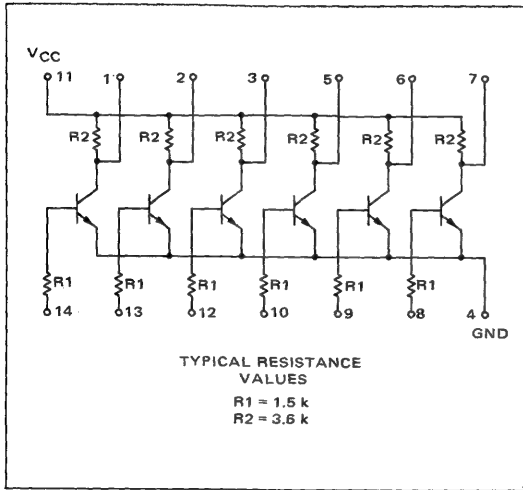
SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



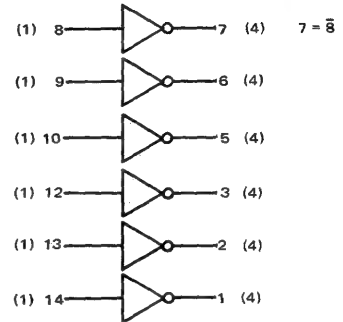
# HEX INVERTERS

PLASTIC mW MRTL MC700P/800P series

## MC9718P • MC9818P

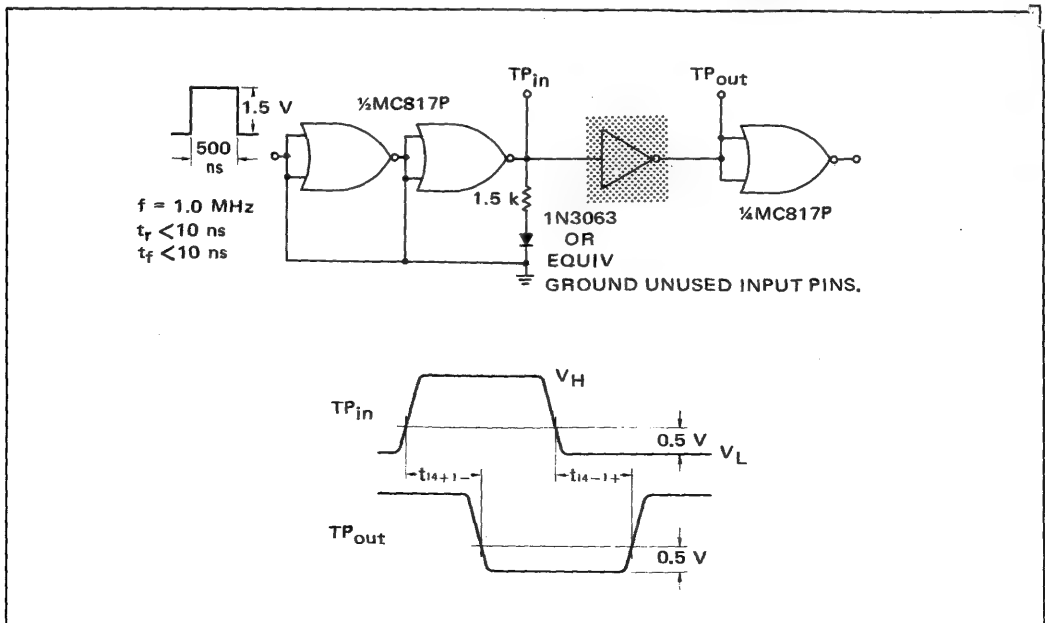


Six individual circuits are contained in a single package. Each provides the simple inversion function.



$t_{pd} = 27\text{ ns}$   
 $P_D = 7.0\text{ mW}$  (Input High) Number In Parenthesis Indicates  
 $3.0\text{ mW}$  (Input Low) Loading Factor

### SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



## ELECTRICAL CHARACTERISTICS

Test procedures are shown for one inverter only.  
The other inverters are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES				
		(Volts)				
		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>
MC9818P	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60
MC9718P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC9818P Test Limits							MC9718P Test Limits							TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	Gnd
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max							
Input Current	I <sub>in</sub>	14*	-	150	-	140	-	140	μA <sub>dc</sub>	-	150	-	150	-	150	μA <sub>dc</sub>	14	-	*	-	11	4
Output Current	I <sub>A4</sub>	1	570	-	570	-	535	-	μA <sub>dc</sub>	570	-	570	-	570	-	μA <sub>dc</sub>	1	-	-	14	11	4
Output Voltage	V <sub>out</sub>	1	-	400	-	350	-	300	mV <sub>dc</sub>	-	400	-	300	-	320	mV <sub>dc</sub>	-	14	-	-	11	4
Saturation Voltage	V <sub>CE(sat)</sub>	1	-	250	-	250	-	250	mV <sub>dc</sub>	-	220	-	230	-	320	mV <sub>dc</sub>	-	-	14	-	11	4
Switching Time	t <sub>on</sub> + t <sub>off</sub>	1, 14	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	Pulse In	Pulse Out	-	-	11	4
																	14	1				

Ground inputs of inverters not under test. Other pins not listed are left open

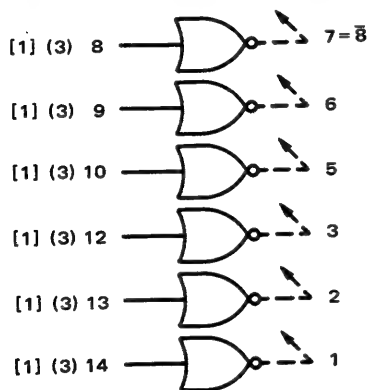
\* To simulate worse case conditions, the output of inverter under test is tied to the output of another inverter which has its input taken to V<sub>BOT</sub>.

# HEX EXPANDERS

PLASTIC MRTL MC700P/800P series

## MC9719P • MC9819P

Six individual expanders are contained in a single package to increase the input capability of MRTL gates.

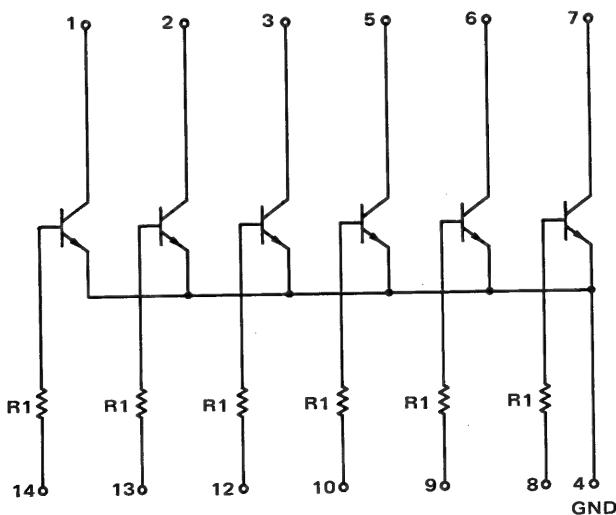


$t_{pd} = 12 \text{ ns}$   
 $P_D = 13 \text{ mW typ (Input High)}$   
 Negligible (Inputs Low)

NUMBER IN PARENTHESES  
 INDICATES mW MRTL LOADING FACTOR

NUMBER IN BRACKETS  
 INDICATES MRTL LOADING FACTOR

When an expander is added to a gate, subtract 0.4 load from the output of the gate for each expander circuit added.  
 SEE GENERAL INFORMATION SECTION FOR EXPANDER RULES



$V_{CC}$  connection to pin 11 is not shown  
 Typical Resistance Value  
 $R1 = 450 \Omega$

# ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.  
The other expanders are tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC9819P Test Limits							MC9719P Test Limits							TEST VOLTAGE							Gnd
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	APPLIED TO PINS LISTED BELOW:							
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	V <sub>R</sub> *		
Input Current	I <sub>in</sub>	14	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	14	-	-	-	11	1	4	
Output Leakage Current	I <sub>CEX</sub>	1	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	1	-	-	14	11	-	4	
Output Voltage	V <sub>out</sub>	1	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	14	-	-	11	1	4	
Saturation Voltage	V <sub>CE(sat)</sub>	1	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	14	-	11	1	4	

Ground inputs of expanders not under test. Other pins not listed are not tested.

Ground inputs of expanders not under test. Other pins not listed are left open.

\* Resistor value to V<sub>CC</sub>

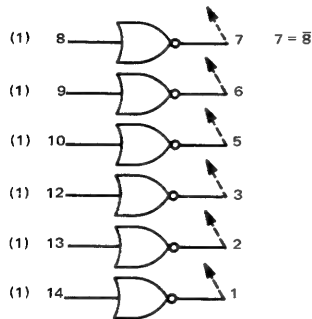
@ Test Temperature		TEST VOLTAGE VALUES					
		(Volts)					(Ohms)
		V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	V <sub>R</sub> *
MC9819P	0°C	0.980	0.930	1.80	0.570	3.60	640
	+25°C	0.910	0.880	1.80	0.500	3.60	640
	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC9719P	+15°C	0.865	0.865	1.80	0.475	3.60	640
	+25°C	0.850	0.850	1.80	0.460	3.60	640
	+55°C	0.800	0.800	1.80	0.430	3.60	640

# HEX EXPANDERS

## PLASTIC mW MRTL MC700P/800P series

### MC9720P • MC9820P

Six individual expanders are contained in a single package to increase the input capability of the mW MRTL gates.

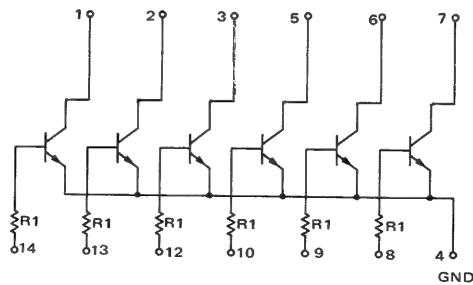


$t_{pd} = 12 \text{ ns}$   
 $P_D = 30 \text{ mW}$  (Inputs High)  
 Negligible (Inputs Low)

Number In Parenthesis Indicates Loading Factor.

#### NOTES ON THE USE OF THE MC9720/9820

1. The input loading factor of the expanded gate is 1.33.
2. Pin 11 of the expander must be connected to  $V_{CC}$ .
3. The output loading factor of the expander gate is decreased 0.5 load for every added node.



CONNECTION TO  $V_{CC}$  NOT SHOWN  
 TYPICAL RESISTANCE  
 VALUES  
 $R1 = 1.5 \text{ k}\Omega$



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.  
The other expanders are tested in the same manner.

@ Test  
Temperature

MC9820P

MC9720P

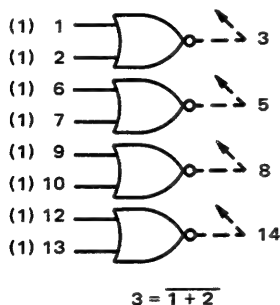
TEST VOLTAGE VALUES						Gnd
(Volts)					(k Ohms)	
V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	V <sub>R</sub> *	
0.880	0.850	1.80	0.500	3.60	3.6	
0.830	0.800	1.80	0.460	3.60	3.6	
0.740	0.710	1.80	0.400	3.60	4.0	
0.865	0.865	1.80	0.475	3.60	3.6	
0.850	0.850	1.80	0.460	3.60	3.6	
0.800	0.800	1.80	0.430	3.60	3.6	
TEST VOLTAGE APPLIED TO PINS LISTED BELOW:						Gnd
V <sub>in</sub>	V <sub>on</sub>	V <sub>BOT</sub>	V <sub>off</sub>	V <sub>CC</sub>	V <sub>R</sub> *	
14	-	-	-	11	1	
1	-	-	14	11	-	
-	14	-	-	11	1	
-	-	14	-	11	1	

Characteristic	Symbol	Pin Under Test	MC9820P Test Limits							MC9720P Test Limits						
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max	
Input Current	I <sub>in</sub>	14	-	150	-	140	-	140	μA <sub>dc</sub>	-	150	-	150	-	150	μA <sub>dc</sub>
Output Leakage Current	I <sub>CEX</sub>	1	-	25	-	25	-	30	μA <sub>dc</sub>	-	40	-	40	-	50	μA <sub>dc</sub>
Output Voltage	V <sub>out</sub>	1	-	400	-	350	-	300	mV <sub>dc</sub>	-	400	-	300	-	320	mV <sub>dc</sub>
Saturation Voltage	V <sub>CE(sat)</sub>	1	-	250	-	250	-	250	mV <sub>dc</sub>	-	220	-	230	-	320	mV <sub>dc</sub>

Ground unused input pins. Other pins not listed are left open. \*Resistor value to V<sub>CC</sub>.

**MC9721P • MC9821P**

Four 2-input expanders housed in a single package increase the input capability of mW MRTL gates.



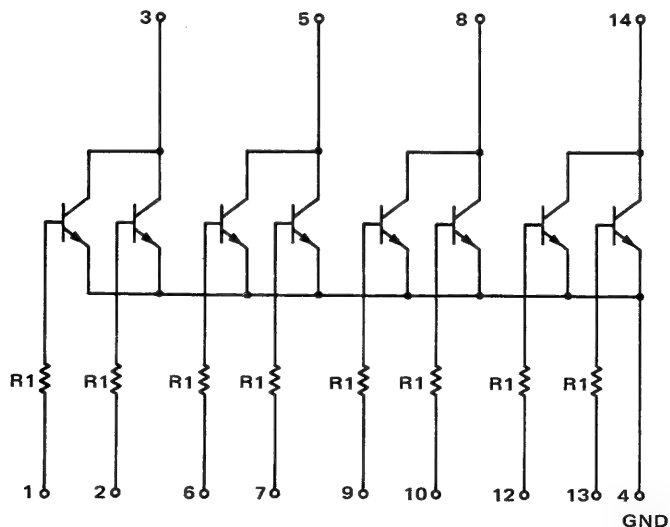
NUMBER IN PARENTHESIS INDICATES  
LOADING FACTOR

**NOTES ON THE USE OF THE MC9721/MC9821**

1. The input loading factor of the expanded gate is 1.33.
2. Pin 11 of the expander must be connected to  $V_{CC}$ .
3. The output loading factor of the expanded gate is decreased 0.5 load for every added node.

$t_{pd} = 27 \text{ ns}$

$P_D = 20 \text{ mW typ (Input High)}$   
Negligible (Inputs Low)



$V_{CC}$  connection to pin 11 is not shown  
Typical Resistance Values  
 $R1 = 1.5 \text{ k}$

# ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.  
The other expanders are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES						
		(Volts)					(k $\Omega$ )	
		V <sub>in</sub>	V <sub>on</sub>	V <sub>BoT</sub>	V <sub>off</sub>	V <sub>CC</sub>	V <sub>R</sub> *	
MC9821P	0°C	0.880	0.850	1.80	0.500	3.60	3.6	
	+25°C	0.830	0.800	1.80	0.460	3.60	3.6	
	+75°C	0.740	0.710	1.80	0.400	3.60	4.0	
MC9721P	+15°C	0.865	0.865	1.80	0.475	3.60	3.6	
	+25°C	0.850	0.850	1.80	0.460	3.60	3.6	
	+55°C	0.800	0.800	1.80	0.430	3.60	3.6	

Characteristic	Symbol	Fin Under Test	MC9821P Test Limits							MC9721P Test Limits							TEST VOLTAGE						Gnd
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	APPLIED TO PINS LISTED BELOW:						
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		Min	Max	V <sub>IN</sub>	V <sub>ON</sub>	V <sub>BOT</sub>	V <sub>OFF</sub>	
Input Current	I <sub>in</sub>	1	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	1	-	2	-	11	3	4
		2	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	2	-	1	-	11	3	4
Output Leakage Current	I <sub>CEX</sub>	3	-	25	-	25	-	30	μAdc	-	40	-	40	-	50	μAdc	3	-	-	1,2	11	-	4
Output Voltage	V <sub>out</sub>	3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	3	2,4
		3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	2	-	-	11	3	1,4
Saturation Voltage	V <sub>CE(sat)</sub>	3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	1	-	11	3	2,4
		3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	2	-	11	3	1,4

Ground unused input pins. Other pins not listed are left open.

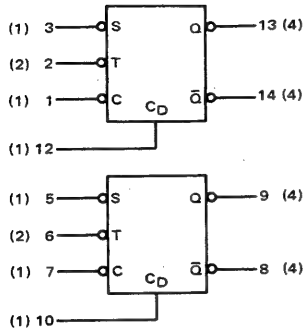
\* Resistor value to V<sub>CC</sub>.

# DUAL J-K FLIP-FLOPS

PLASTIC mW MRTL MC700P/800P series

## MC9722P • MC9822P

MC9722P/9822P consists of two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



NUMBER IN PARENTHESIS INDICATES LOADING FACTOR

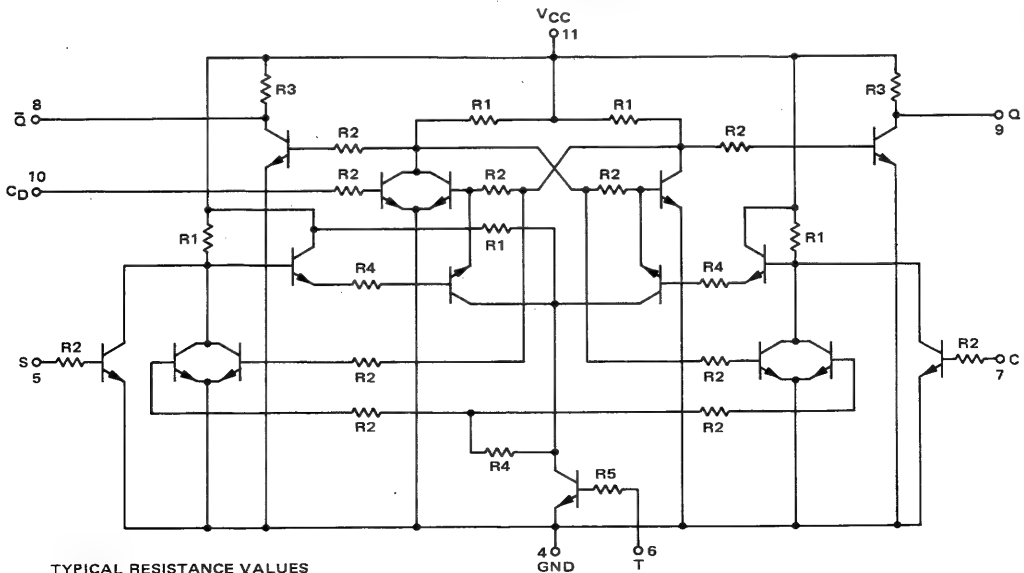
### CLOCKED INPUT OPERATION ①

$t_n$ ②	$t_{n+1}$ ②		
S	C	Q	$\bar{Q}$
1	1	$Q_n$ ③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	$Q_n$ ③

$f_{Tog} = 4.0 \text{ MHz}$   
 $t_{pd} = 75 \text{ ns typ}$   
 $P_D = 24 \text{ mW typ (Only Clock Input High)}$

1. Direct input ( $C_D$ ) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted  $t_n$  and the time period subsequent to this transition is denoted  $t_{n+1}$ .
3.  $Q_n$  is the state of the Q output in the time period  $t_n$ .

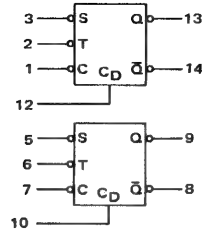
### 1/2 OF CIRCUIT SHOWN



TYPICAL RESISTANCE VALUES  
 $R1 = 4.5 \text{ k}$   
 $R2 = 1.5 \text{ k}$   
 $R3 = 3.6 \text{ k}$   
 $R4 = 2.0 \text{ k}$   
 $R5 = 750\Omega$

# ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only. The other flip-flop is tested in the same manner.



@ Test Temperature  
MC9822P { 0°C  
+25°C  
+75°C  
MC9722P { +15°C  
+25°C  
+55°C

TEST VOLTAGE VALUES						
Volts					Pulse	
$V_{in}$	$V_{on}$	$V_{BOT}$	$V_{off}$	$V_{CC}$	$C_P$	
0.880	0.850	1.80	0.500	3.60	$V_{in}$ to $V_{off}$	
0.830	0.800	1.80	0.460	3.60	$V_{in}$ to $V_{off}$	
0.740	0.710	1.80	0.400	3.60	$V_{in}$ to $V_{off}$	
0.865	0.865	1.80	0.475	3.60	$V_{in}$ to $V_{off}$	
0.850	0.850	1.80	0.460	3.60	$V_{in}$ to $V_{off}$	
0.800	0.800	1.80	0.430	3.60	$V_{in}$ to $V_{off}$	
TEST VOLTAGE APPLIED TO PINS LISTED BELOW:						
$V_{in}$	$V_{on}$	$V_{BOT}$	$V_{off}$	$V_{CC}$	$C_P$	Gnd
5	-	10	-	11	-	4
7	-	-	-	-	-	-
10	-	-	-	-	-	-
6	-	5,7	-	↓	-	↓
-	8,10	-	-	11	-	4
-	9	-	-	11	-	4
$P_{in\ 1}$	$P_{in\ 2}$		$P_{in\ 3}$			
5	-	6	7	11	-	4,10
5	7	↓	-	↓	-	↓
-	-	-	5	-	7	-
-	5	-	-	-	7	-
5	7	-	-	-	-	-
5	-	-	7	-	-	-
-	5	-	-	-	7	-
-	-	↓	5	↓	7	↓

Ground inputs of flip-flop not under test. Other pins not listed are left open.

- \*Preset the device as follows:
- Momentarily apply V<sub>BOT</sub> to pin 10, this preclears the flip-flop.
  - Remove V<sub>BOT</sub>, ground pins 5 and 7.
  - Apply negative-going clock pulse (C<sub>p</sub>) to pin 5 while pins 5 and 7 are still grounded. (This changes the state of the flip-flop to a set condition.)
  - Remove ground from pins 5 and 7.

\*\*Apply V<sub>BOT</sub> momentarily prior to arrival of clock pulse (C<sub>p</sub>) to change the state of the flip-flop.

- ④ See Figure 4
- ⑤ See Figure 5
- ⑥ See Figure 6
- ⑦ See Figure 7

(continued)



MC9722P, MC9822P (continued)

FIGURE 1 – CLOCK PULSE DEFINITION

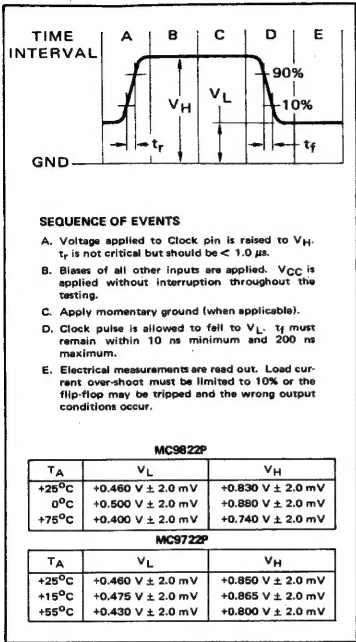


FIGURE 2 – TOGGLE MODE TEST CIRCUIT

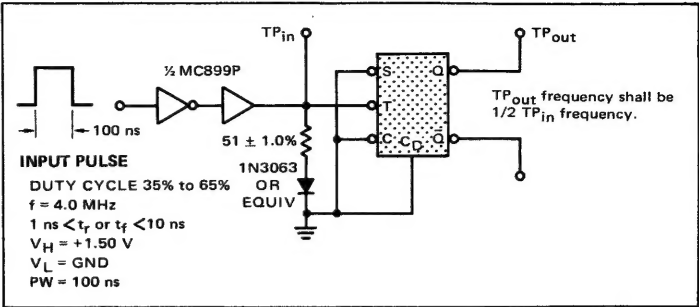


FIGURE 3 – TEST CIRCUIT

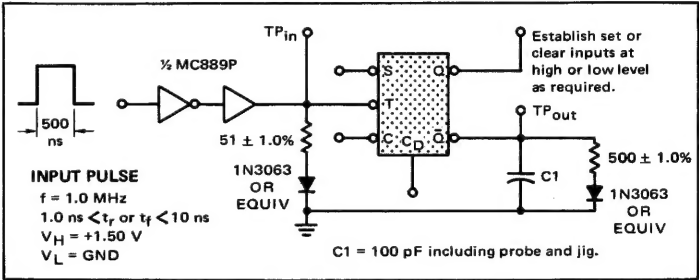


FIGURE 4 – TEST WAVEFORMS

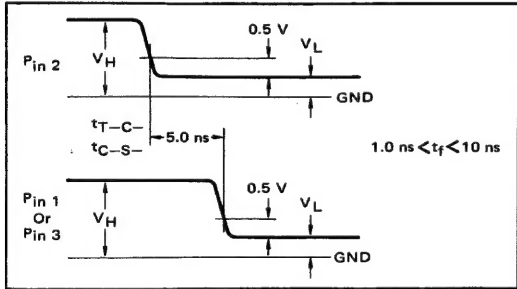


FIGURE 5 – TEST WAVEFORMS

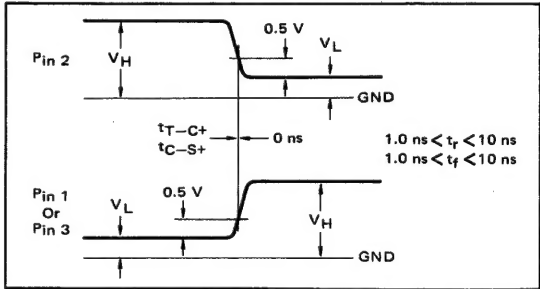


FIGURE 6 – TEST WAVEFORMS

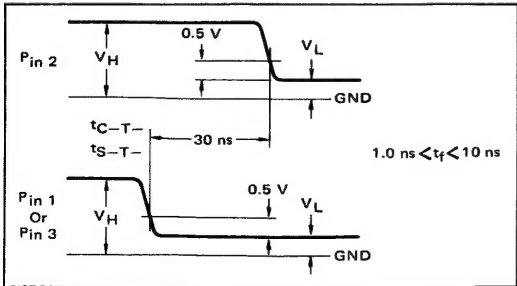
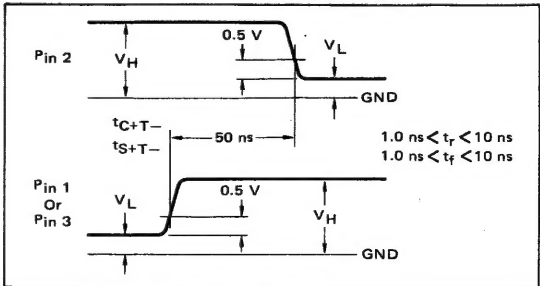


FIGURE 7 – TEST WAVEFORMS



BCD-TO-DECIMAL  
DECODER-DRIVER

PLASTIC MRTL MC700P/800P series

MC9760P • MC9860P†

The MC9760P/MC9860P monolithic BCD-to-Decimal Decoder/Driver is designed for use with high-voltage neon indicating tubes. The high-voltage output transistors can withstand 70-volts (MC9860P), and 65-volts (MC9760P), insuring direct operation of the indicator tubes without back-ground glow. The inputs are compatible with MRTL logic functions.

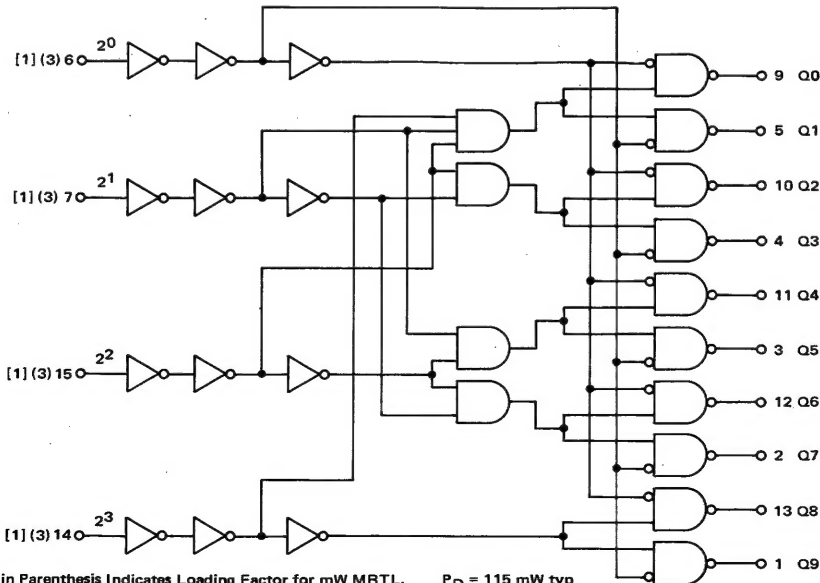
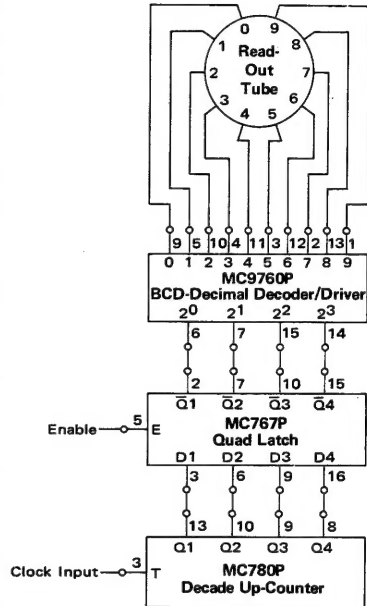
TRUTH TABLE

Value Pin No. Logic Levels	INPUT* (BCD)				OUTPUT (DECIMAL)									
	2 <sup>0</sup>	2 <sup>1</sup>	2 <sup>2</sup>	2 <sup>3</sup>	0	1	2	3	4	5	6	7	8	9
	6	7	15	14	9	5	10	4	11	3	12	2	13	1
1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	0	1	1	1	1	1	1	1
0	1	0	1	1	1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	0	1	1	1	1	1	1
0	1	1	0	1	1	1	1	0	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	0	1	1	1	1	1
0	1	0	0	1	1	1	1	1	0	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1	0	1	1	1	1
0	1	1	1	0	1	1	1	1	1	0	1	1	1	1

Logic "0"  $\leq 1.5$  Vdc @ 6.0 mA  
Logic "1"  $\geq 65$  Vdc (MC9760)  
Logic "1"  $\geq 70$  Vdc (MC9860)

\*Any input configuration not shown results in an indeterminate state at the outputs.

TYPICAL INTERCONNECTION  
DIAGRAM

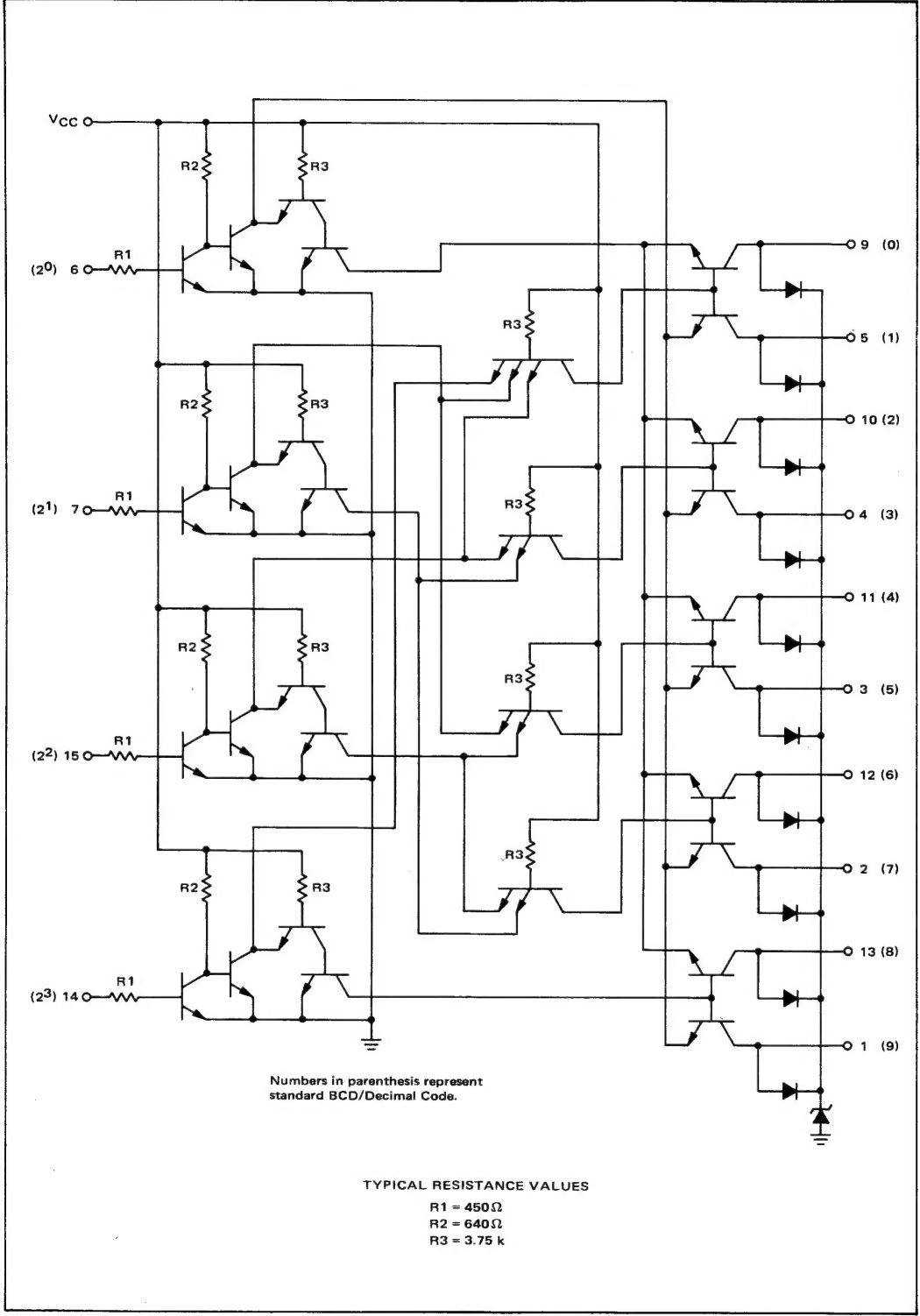


Number in Parenthesis Indicates Loading Factor for mW MRTL.  
Number in Brackets Indicates Loading Factor for MRTL.

†See General Information section for packaging.



MC9760P, MC9860P (continued)



## ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS										@ Test Temperature		TEST VOLTAGE/CURRENT VALUES (Vdc/mAdc)						TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW						Gnd
Characteristic	Symbol	Pin Under Test	MC9860P Test Limits						MC9760P Test Limits						V <sub>in</sub>	V <sub>on</sub>	V <sub>CEX</sub>							
			0°C		+25°C		+75°C		Unit	+15°C		+25°C		+55°C		Unit	V <sub>in</sub>	V <sub>on</sub>	V <sub>CEX</sub>	I <sub>A</sub>	I <sub>L</sub>	V <sub>CC</sub>		
Min	Max	Min	Max	Min	Max	Min	Max	Min		Max	Min	Max	Min	Max	Min								Max	
Input Current	I <sub>in</sub>	6 7 14 15	- - - ↓	600 - - ↓	- - - ↓	600 - - ↓	- - - ↓	570 - - ↓	μAdc ↓	- - - ↓	500 - - ↓	- - - ↓	500 - - ↓	- - - ↓	470 - - ↓	μAdc ↓	6 7 14 15	- - - -	- - - -	- - - -	- - - -	16 ↓	8 ↓	
Output Voltage	V <sub>out</sub>	1	-	1.5	-	1.5	-	1.5	Vdc	-	1.5	-	1.5	-	1.5	Vdc	-	*	-	1	-	16	8*	
Output Leakage Current	I <sub>CEX</sub>	1	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc	-	**	1	-	-	16	8**	
Output Breakdown Voltage	BV <sub>CEX</sub>	1 2 3 4 5 9 10 11 12 13	70 ↓ - - - - - - - ↓	- - - - - - - - ↓	70 ↓ - - - - - - ↓	- - - - - - - - ↓	- - - - - - - - ↓	Vdc ↓	65 ↓	- - - - - - - - ↓	65 ↓	- - - - - - - - ↓	- - - - - - - - ↓	65 ↓	- - - - - - - - ↓	Vdc ↓	- 6,7,14,15 ↓ 14,15 ↓	- - - - - - - - ↓	- - - - - - - - ↓	1 2 3 4 5 9 10 11 12 13	16 ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓	8 ↓ 6,7,8 ↓		
Power Supply Current Drain	I <sub>PD</sub>	16	-	-	-	30	-	-	mAdc	-	-	-	30	-	-	mAdc	-	6,7,14,15	-	-	-	16	8	

\*I<sub>A</sub> is applied to pin under test - V<sub>ON</sub> and gnd are applied to inputs in accordance with truth table for "on" condition of pin under test (1 test for each output).

\*\*V<sub>CEX</sub> is applied to pin under test - V<sub>ON</sub> and gnd are applied to inputs in accordance with truth table for "off" conditions of pin under test (9 tests for each output).

Other pins not listed are left open.